DATA SHEET

SAA2501
Digital Audio Broadcast (DAB) decoder

Preliminary specification
File under Integrated Circuits, IC01

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Philips Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- Advanced error protection
- Integrated audio post processing for control of signal level and inter-channel crosstalk
- Demultiplexing of Program Associated Data (PAD) in the input bitstream
- Automatic digital de-emphasis of the decoded audio signal
- Separate master and slave inputs
- Automatic sample frequency and bit-rate switching in master input mode
- Automatic synchronization of input and output interface clocks in master input mode
- Selectable audio output precision; 16, 18, 20 or 22 bit
- Low power consumption
- Decoded sub-band signal and error flag outputs for error concealment.

2 APPLICATION

- Digital Audio Broadcast systems as defined in *"Eureka 147"*.

3 GENERAL DESCRIPTION

The SAA2501 audio source decoder supports ISO/IEC MPEG layers I and II and all DAB specific features as described in *"Eureka 147 draft specification (EU147)"*.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA2501H	QFP44[1]	plastic quad flat package; 44 leads (lead length 1.3 mm); body $10 \times 10 \times 1.75$ mm	SOT307-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

Supply of this *"ISO/IEC 11172-3"* audio standard Layer I or layer II compatible IC does not convey a licence nor imply a right under any patent, or any Industrial or Intellectual Property Right, to use this IC in any ready-to-use electronic product.

5 BLOCK DIAGRAM

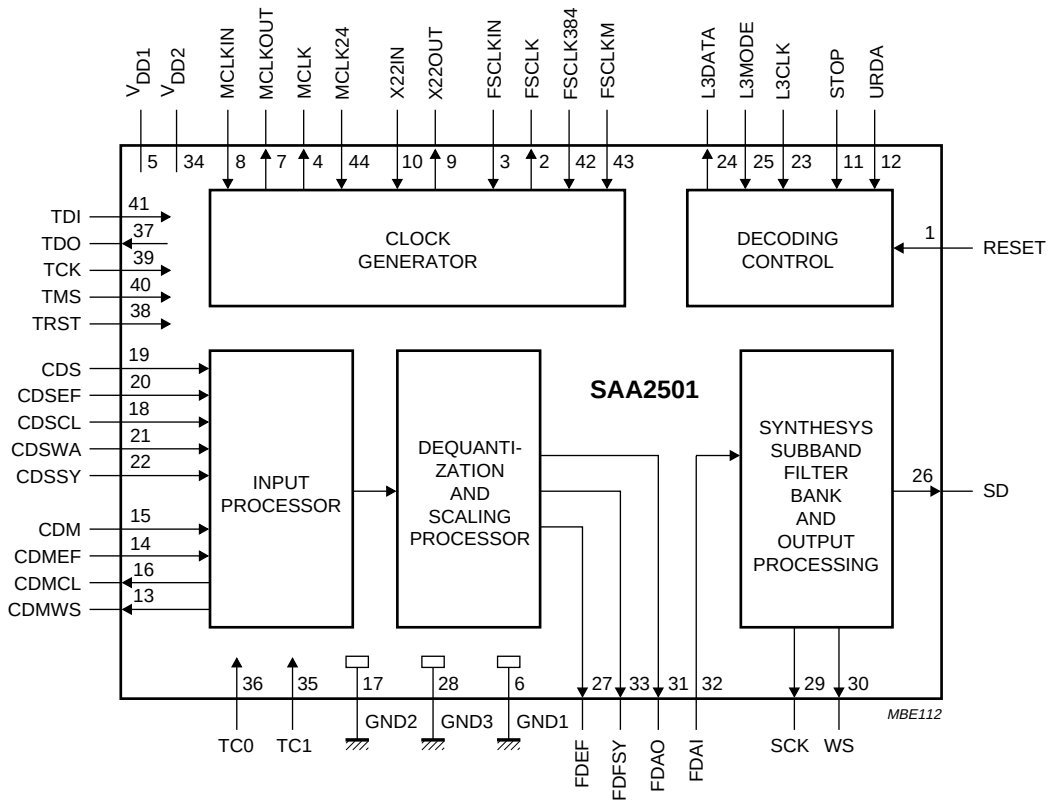


Fig.1 Functional block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION	TYPE
RESET	1	master reset input	I
FSCLK	2	sample rate clock output; buffered signal	O
FSCLKIN	3	sample rate clock signal input (see Table 1)	I
MCLK	4	master clock output; buffered signal	O
V_{DD1}	5	supply voltage 1	–
GND1	6	ground 1	–
MCLKOUT	7	master clock oscillator output	O
MCLKIN	8	master clock oscillator input or signal input	I
X22OUT	9	22.579 MHz clock oscillator output	O
X22IN	10	22.579 MHz clock oscillator input or signal input	I
STOP	11	stop decoding input	I
URDA	12	unreliable data input; interrupt decoding	I
CDMWS	13	coded data (master input) word select output	O
CDMEF	14	coded data (master input) error flag input	I
CDM	15	ISO/MPEG coded data (master input)	I
CDMCL	16	coded data (master input) bit clock output	O
GND2	17	ground 2	–
CDSCL	18	coded data (slave input) bit clock	I
CDS	19	ISO/MPEG or EU147 (see Table 8) coded data (slave input)	I
CDSEF	20	coded data (slave input) error flag	I
CDSWA	21	coded data (slave input) burst window signal	I
CDSSY	22	coded data (slave input) frame sync	I
L3CLK	23	L3 interface bit clock input	I
L3DATA	24	L3 interface serial data input/output	I/O
L3MODE	25	L3 interface address/data select input	I
SD	26	baseband audio I^2S data output	O
FDEF	27	filter data error flag output	O
GND3	28	ground 3	–
SCK	29	baseband audio data I^2S clock output	O
WS	30	baseband audio data I^2S word select output	O
FDAO	31	filter data output	O
FDAI	32	filter data input	I
FDFSY	33	filter data output frame sync	O
V_{DD2}	34	supply voltage 2	–
TC1	35	do not connect; factory test control 1 input, with integrated pull-down resistor	I
TC0	36	do not connect; factory test control 0 input, with integrated pull-down resistor	I
TDO	37	boundary scan test data output	O
TRST	38	boundary scan test reset input; this pin should be connected to ground for normal operation	I
TCK	39	boundary scan test clock input	I

SYMBOL	PIN	DESCRIPTION	TYPE
TMS	40	boundary scan test mode select input	I
TDI	41	boundary scan test data input	I
FSCLK384	42	sample rate clock frequency indication input	I
FSCLKM	43	sample rate clock source selection for the master input	I
MCLK24	44	master clock frequency indication input	I

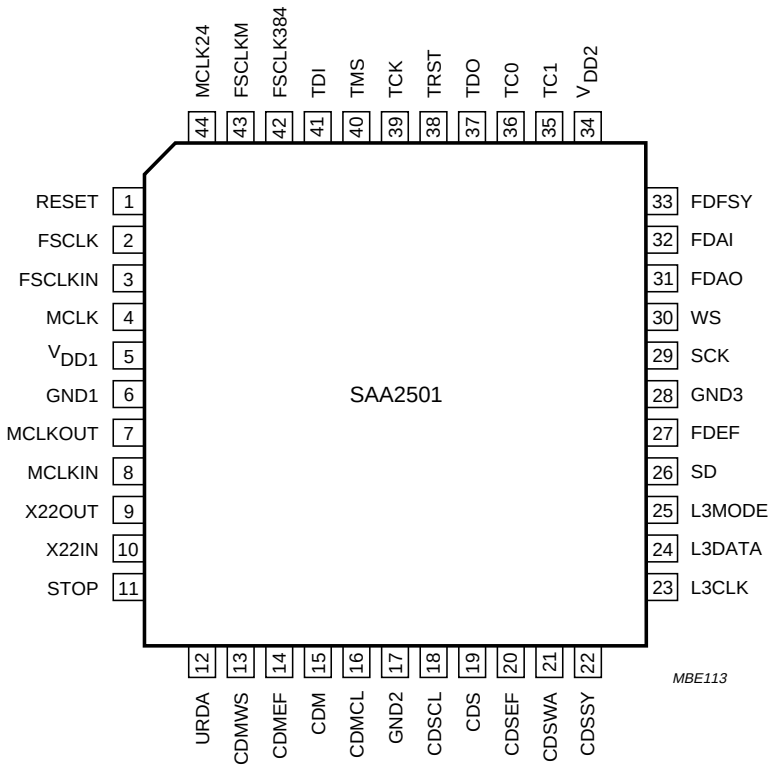


Fig.2 Pin configuration (QFP44).

7 FUNCTIONAL DESCRIPTION

7.1 Coding system

The perceptual audio encoding/decoding scheme defined within the "*ISO/IEC 11172-3 MPEG Standard"* allows for a high reduction in the amount of data needed for digital audio whilst maintaining a high perceived sound quality. The coding is based upon a psycho-acoustic model of the human auditory system. The coding scheme exploits the fact that the human ear does not perceive weak spectral components that are in the proximity (both in time and frequency) of loud components. This phenomenon is called masking.

For layers I and II of ISO/MPEG the broadband audio signal spectrum is split into 32 sub-bands of equal bandwidth. For each sub-band signal a masking threshold is calculated. The sub-band samples are then re-quantized to such an accuracy that the spectral distribution of the re-quantization noise does not exceed the masking threshold. It is this reduction of representation accuracy which yields the data reduction. The re-quantized sub-band signals are multiplexed, together with ancillary information regarding the actual re-quantization, into a MPEG audio bitstream.

During decoding, the SAA2501 de-multiplexes the MPEG audio bitstream, and with knowledge of the ancillary information, reconstructs and combines the sub-band signals into a broadband audio output signal.

7.2 Basic functionality

From a functional point of view, several blocks can be distinguished in the SAA2501. A clock generator section derives the internally and externally required clock signals from its clock inputs. The SAA2501 can switch between a master and a slave input interface to receive the coded input data. The input processor parses and de-multiplexes the input data stream. The de-quantization and scaling processor performs the transformation and scaling operations on the sample representations in the input bitstream to yield sub-band domain samples.

The sub-band samples are transferred via an external detour to the synthesis sub-band filter bank processor. The detour can be used to process the decoded audio in the sub-band domain. The baseband audio samples, reconstructed by the sub-band filter bank, can be processed before being output.

The decoding control block houses the L3 control interface, and handles the response to external control signals. The L3 control interface enables the application to configure the SAA2501, to read its decoding status, to read Program Associated Data, and so on.

Several pins are reserved for Boundary Scan Test and Scan Test purposes.

7.3 SAA2501 clocks

The SAA2501 clock interfacing is designed for application versatility. It consists of 10 signals (see Table 1).

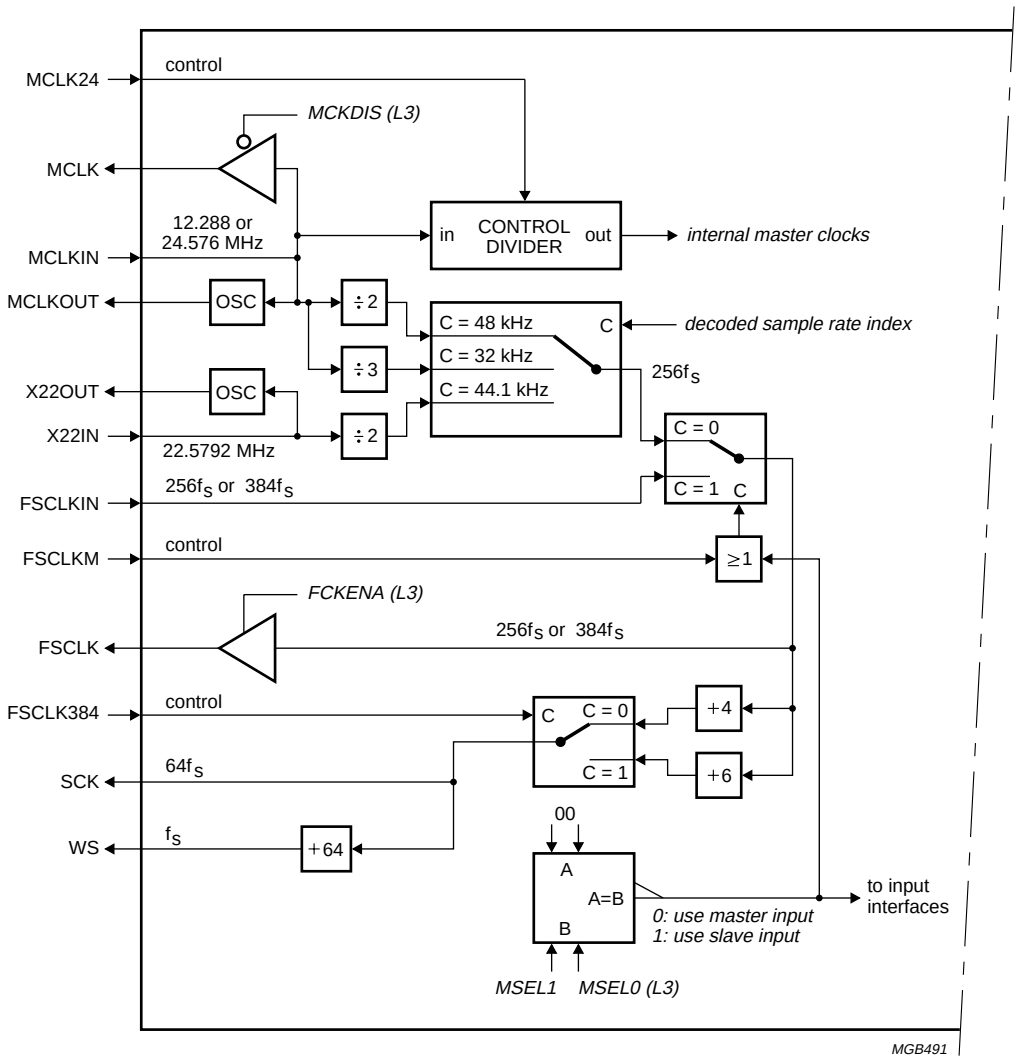
From a functional point of view, the clock generator inside the device can be represented as shown in Fig.3.

As described above, the SAA2501 incorporates a master input interface on which it requests for coded input data itself, as well as a slave input interface for an imposed coded data input bitstream. The input interface is selected with flags MSEL0 and MSEL1, controlled via the L3 microcontroller interface.

Depending on the selected input interface, only a limited number of the three possible input clocks (MCLKIN, X22IN and FSCLKIN) is actually required. The various clock options are selected with the 3 external control signals MCLK24, FSCLKM and FSCLK384. These control signals must be stationary while the device reset signal at pin RESET is de-activated; changing any of these 3 signals without simultaneously resetting the SAA2501 can result in malfunctioning.

Table 1 Clock interfacing signals

SIGNAL	DIRECTION	FUNCTION
MCLKIN	input	master clock oscillator input or signal input
MCLKOUT	output	master clock oscillator output
MCLK	output	master clock output; buffered signal
MCLK24	input	master clock frequency indication input: MCLK24 = 0; MCLKIN frequency is 12.288 MHz (256×48 kHz) MCLK24 = 1; MCLKIN frequency is 24.576 MHz (512×48 kHz)
X22IN	input	22.5792 MHz (512×44.1 kHz) clock oscillator input or signal input
X22OUT	output	22.5792 MHz (512×44.1 kHz) clock oscillator output
FSCLKIN	input	sample rate clock signal input
FSCLK	output	sample rate clock signal input; buffered signal
FSCLK384	input	sample rate clock signal frequency indication input: FSCLK384 = 0; FSCLKIN frequency is $256f_s$ FSCLK384 = 1; FSCLKIN frequency is $384f_s$
FSCLKM	input	sample rate clock source selection when using the master input: FSCLKM = 0; use MCLKIN or X22IN as source FSCLKM = 1; use FSCLKIN as source

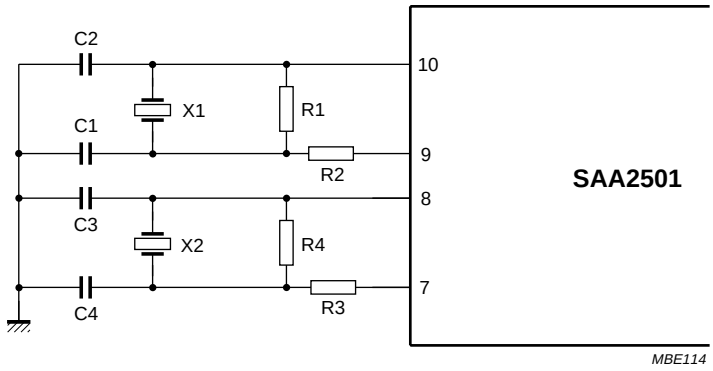


Italics: internal signal designation.

Fig.3 SAA2501 clock generator.

7.4 Crystal oscillator

The recommended crystal oscillator configuration is shown in Fig.4. The specified component values only apply to crystals with a low equivalent series resistance of <40 Ω.



C1 = C2 = 33 pF;
R1 = R4 = 1 MΩ;
R2 = R3 = 1 kΩ;
X1 = 22.5792 MHz;
X2 = 24.5760 MHz or 12.2880 MHz

The specified component values only apply to crystals with a low equivalent series resistance of <40 Ω.

Fig.4 Crystal oscillator components.

7.5 Clock frequencies when using the slave input

If the slave input is used (MSEL1 and MSEL0 = 10 or 11), the SAA2501 clock sources are MCLKIN and FSCLKIN and X22IN is not used. The I^2S clocks SCK and WS are generated by the SAA2501 from FSCLKIN. FSCLKIN may be designated to have a frequency of 256 times (indicated by FSCLK384 = 0) or 384 times (indicated by FSCLK384 = 1) the sample frequency of the coded input data. Master clock signal MCLKIN may be chosen to have a frequency of 12.288 MHz (indicated by MCLK24 = 0) or 24.576 MHz (indicated by MCLK24 = 1). MCLKIN and FSCLKIN do not have to be phase or frequency locked. If the application is based on a sample frequency of 48 kHz or 32 kHz, and a sample rate related clock of 12.288 MHz (256×48 kHz; 384×32 kHz) is available, this can be taken advantage of by using this signal for both MCLKIN and FSCLKIN.

7.6 Clock frequencies when using the master input

If the master input is used (MSEL1 and MSEL0 = 00), one out of two configurations is selected with signal FSCLKM with respect to the clock sources:

1. If FSCLKM = 0, MCLKIN and X22IN are the clock sources. FSCLKIN is not used in this configuration. FSCLK384 must be set to logic 0 for reasons of internal connections in the clock generator circuitry. MCLKIN may have only frequency 24.576 MHz (so mandatory accompanied by MCLK24 = 1), and X22IN must have a frequency of 22.5792 MHz. MCLKIN and X22IN do not have to be phase or frequency locked. The main advantage of this configuration is that the SAA2501 determines automatically which sample rate is active from the sampling rate setting of the input data bitstream, and then selects either MCLKIN or X22IN as the clock source for the I^2S clocks SCK and WS. This configuration is therefore particularly suited in applications with more than one possible sample rate setting.
2. If FSCLKM = 1, the configuration is comparable to the configuration when using the slave input (see Section 7.5). MCLKIN and FSCLKIN are used as the clock sources, and X22IN is not required. MCLKIN may again have a frequency of 12.288 MHz (indicated by MCLK24 = 0) or 24.576 MHz (indicated by MCLK24 = 1), and FSCLKIN may have a frequency of 256 times (indicated by FSCLK384 = 0) or 384 times (indicated by FSCLK384 = 1) the sample frequency of the input data. MCLKIN and FSCLKIN do not have to be phase or frequency locked.

7.7 Target applications; applying the SAA2501 with 2 ISO/MPEG sources

In Table 2 the three target applications of the SAA2501 are summarised. The slave input application is labelled S, and the master input applications are labelled M0 and M1.

Table 2 Target applications

ATTRIBUTE CONDITIONS		APPLICATION		
		SLAVE INPUT	MASTER INPUT	
INPUT INTERFACE	**CONDITIONS**	**S**(1)	**M0**(2)	**M1**
FSCLKM		X	0	1
MCLKIN	MCLK24 = 1	24.576 MHz	24.576 MHz	24.576 MHz
	MCLK24 = 0	12.288 MHz	illegal	12.288 MHz
X22IN		note 3	22.579 MHz	note 3
FSCLKIN	FSCLK384 = 1	$384f_s$	illegal	$384f_s$
	FSCLK384 = 0	$256f_s$	note 3	$256f_s$
FSCLK	FCKENA = 1 (L3)	copy of FSCLKIN	$256f_s$	copy of FSCLKIN

Notes

1. FSCLKIN must be locked to input data clock CDSCL; see Section 7.17.2.
2. FSCLKIN is not used, but FSCLK384 must be LOW.
3. Must be electrically defined; e.g. LOW.

Sections 7.5 and 7.6 explain which clock sources are activated by the SAA2501 depending on the selected input interface. This automatic clock source selection makes it easy to apply the SAA2501 in systems with two ISO/MPEG coded data sources (one connected to the master input, an one to the slave input), even if these data sources use different clocks.

7.8 Buffered clock outputs

The SAA2501 provides a signal MCLK which is a buffered version of MCLKIN. MCLK can be set to 3-state by setting the L3 control interface flag MCKDIS to 1 in applications where MCLK is not needed.

Signal FSCLK is copied from the FSCLKIN input for application types S and M1 or generated with a frequency of $256f_s$ by the SAA2501 for application type M0. After a device reset, FSCLK must be enabled explicitly by setting L3 flag FCKENA, or can alternatively be left 3-stated in applications where it is not needed.

After a device reset, MCLK is enabled; FSCLK is disabled (i.e. both MCKDIS and FCKENA are set to logic 0).

7.9 Functionality issues

The SAA2501 fully complies with ISO/MPEG layer I and II and EU147 with the slave input. With the master input, the SAA2501 complies with ISO/MPEG layer I and II, excluding the free format bit rate. Several aspects of the decoding process, as well as the audio post-processing features, offered by the SAA2501, are described in more detail in Section 7.10.

7.10 Synchronization to input data bitstreams

After a reset, the SAA2501 mutes both sub-band and baseband audio data. After data inputting has started, the SAA2501 searches either for a sync pattern or a sync pulse. The speed at which input data is read by the master input to search for synchronization is described below. If the application is such that the SAA2501 starts at a random moment in time compared to the bitstream, maximal one frame is skipped before a synchronization pattern or pulse is encountered.

When the SAA2501 has detected the first synchronization word or pulse, a number of frames are decoded in order to verify synchronization; the input data for these frames is read and decoded, but meanwhile the audio output is muted. The number of muted frames depends on the input data format (ISO/MPEG or EU147), whether the ISO/MPEG Cyclic Redundancy Check (CRC) is active, and whether the bit rate is free format. If the synchronization is found to be false, the SAA2501 resumes the initial synchronization as described above. If the detected pulse/pattern is concluded to be a real synchronization pulse/pattern, Table 3 indicates the number of muted frames.

Table 3 Muted frames

CRC	MINIMUM NUMBER OF MUTED FRAMES DURING SYNCHRONIZATION	
	FREE FORMAT BIT RATE	NON-FREE-FORMAT BIT RATE
No CRC	2	1
CRC	1	0

7.11 Master input bit rate selection

As explained in Section 7.10, the SAA2501 can be used to alternate between two applications: one with the slave input, and one with the master input. When using the master input, the SAA2501 should fetch data with the effective bit rate, but cannot know what the bit rate of the input data is until it has established synchronization. To overcome this paradox, the input requesting is done at the last selected bit rate.

After a device reset, the master input bit rate selection defaults to the value indicated in Table 4.

Table 4 Defaults master input bit rate

FSCLKM	FSCLK384	FSCLKIN	DEFAULT MASTER INPUT BIT RATE (kbits/s)
0	0	X[1]	384
1	0	256 × 32 kHz	278.64
	1	384 × 32 kHz	
	0	256 × 44.1 kHz	384
	1	384 × 44.1 kHz	
	0	256 × 48 kHz	417.96
	1	384 × 48 kHz	

Note

1. X = don't care.

When FSCLKM = 0, the default master input bit rate is 384 kbits/s. When FSCLKM = 1, the SAA2501 uses signal FSCLKIN to derive the selected bit rate, but it has no indication concerning the sample rate corresponding to FSCLKIN. Therefore, a bit rate of 384 kbits/s is selected at an assumed sample rate of 44.1 kHz; with other sample rates, the bit rate changes proportionally.

The consequence is that while the SAA2501 synchronises (e.g. after a device reset), the application must at least be able to supply at the given default bit rate the required number of frames plus one additional frame (because of the random decoding start point in the input bitstream). Buffers in the application must thus be chosen sufficiently large to prevent under or overflows.

The speed with which input data is requested by the master input is changed by the SAA2501 in each of the following cases:

1. When input synchronization is established after checking a number of frames and the bit rate index of the newly decoded bitstream indicates a different bit rate than that currently selected. In this event, the bit rate is adapted to the newly decoded index.
2. When the active input interface is changed from the master to the slave input, or the signal STOP is activated; in these events input requesting stops.
3. When the active input interface is changed from the slave to the master input, or the signal STOP is deactivated; the bit rate is set to the last selected master input bit rate (the last selected master input bit rate is memorised while using the slave input).

In all other events (e.g. when the SAA2501 goes and stays out of synchronization), the data requesting speed of the master input is maintained.

7.12 Sample rate selection

When using the slave input, or when using the master input with FSCLKM = 1, the application must know the sample rate: FSCLKIN must be applied, which has a frequency which is a multiple of the sample rate; the (sample rate dependent) I^2S timing signals SCK and WS are generated from FSCLKIN. These configurations will normally be used in applications with a fixed sample rate. Should the sample rate change, then the SAA2501 must be reset.

When using the master input with FSCLKM = 0, the SAA2501 selects the active sample rate autonomously, and generates the signals SCK and WS from its crystal clocks. After a device reset, the SAA2501 selects a sample rate of 44.1 kHz by default.

SCK and WS may, and will only, show phase or frequency changes in any of the following 3 situations:

1. When the SAA2501 establishes synchronization with the coded data input bitstream.
2. When the active input interface is changed from the master input with FSCLKM = 0 to the slave input (i.e. the timing source for the generation of SCK and WS is switched from the crystal clocks to FSCLKIN).
3. When the active input interface is changed from the slave input to the master input with FSCLKM = 0 (i.e. the timing source for the generation of SCK and WS is switched from FSCLKIN to the crystal clocks); the sample rate is set to the last selected sample rate that was used with the master input (the last selected sample rate is memorized while using the slave input).

In all other cases, SCK and WS keep on running without phase or frequency changes, and the sample rate selection remains unchanged.

7.13 Handling of errors in the coded input data

The SAA2501 can handle errors in the input data. Errors are assumed to be present in 3 events:

1. If errors are indicated with the coded input data error flag CDSEF and/or CDMEF.
2. On CRC failure if ISO/MPEG error protection is active.
3. If input bitstream syntax errors are detected.

Errors in the input data have an effect on the decoding process if the corrupted data is inside the header, bit allocation or scale factor select information field in a frame (then the SAA2501 will mute) or inside the scale factor field (then the previous scale factor will be copied). Errors in other data fields are not handled explicitly. If the ISO/MPEG CRC is active, only the CRC result is interpreted: CDSEF/CDMEF un-reliability indications for bit allocation and scale factor select information are neglected.

In applications where the ISO/MPEG CRC is always present, the protection bit (which itself is not protected) in the ISO/MPEG header may be overruled by making L3 settings flag CRCACT HIGH. In this manner, the SAA2501 is made robust for data errors on the protection bit.

7.14 Sub-band filter signals

The decoded sub-band signals are output, together with an error indication so that concealment can be applied externally. The optionally concealed sub-band signals are put back into the SAA2501 for synthesis filtering.

7.15 Baseband audio processing

The baseband audio de-emphasis as indicated in the ISO/MPEG input data is performed digitally inside the SAA2501. The incorporated ‘Audio Processing Unit’ (APU) (see Fig.5) can be used to apply inter-channel crosstalk or independent volume control per channel. The APU attenuation coefficients LL, LR, RL and RR may be changed dynamically by the host microcontroller, writing their 8-bit indices to the SAA2501 over the L3 control bus. The coefficient changes become effective within one sample period after the coefficient index writing.

To avoid clicks at coefficient changes, the transition from the current attenuation to the next is smoothed. The relation between the APU coefficient index and the actual coefficient (i.e. the gain) is given in Table 5.

Table 5 APU coefficient index and actual coefficient

APU COEFFICIENT INDEX C		APU COEFFICIENT
BINARY	DECIMAL	
00000000 to 00111111	0 to 63	$2^{-\frac{C}{12}}$
01000000 to 01111110	64 to 126	$2^{-\frac{C-32}{6}}$
01111111	127	0
1XXXXXXX	128 to 255	reserved

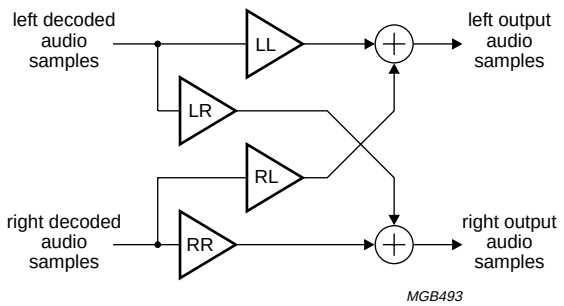


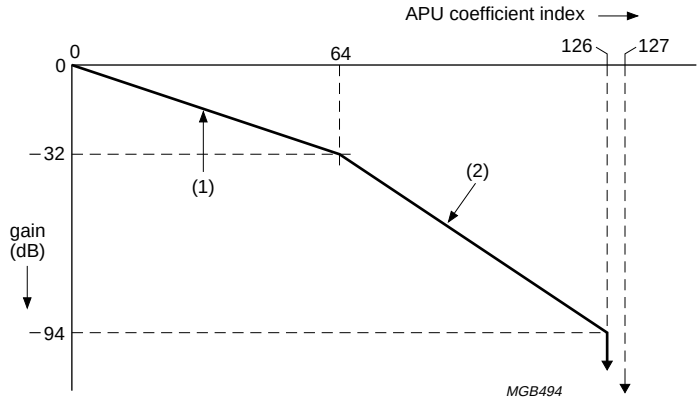
Fig.5 Audio Processing Unit (APU).

From Table 5 we learned that up to coefficient index 64 the step size is approximately –0.5 dB per coefficient increment, and from coefficient index 64 to index 126 the step size is approximately –1 dB per increment.

Note that the APU has no built-in overflow protection, so the application must take care that the output signals of the APU cannot exceed 0 dB level. For an update of the APU coefficients, it may be required to increase some of the coefficients and decrease some others. The APU coefficients are always written sequentially in the fixed sequence LL, LR, RL and RR. Therefore, to prevent internal APU data overflow due to non-simultaneous coefficient updating, the following steps can be followed:

1. Write LL, LR, RL, RR once, but change only those coefficients that must decrease; overwrite the coefficients that must increase with their old value (so do not change these yet).
2. Write LL, LR, RL, RR again, but now change those coefficients that must increase, keeping the other coefficients unchanged.

The consequence of this two-pass coefficient updating is that the application must keep a shadow of the current APU coefficients (the L3 APU coefficients data item is write-only).



(1) Step –0.5 dB per coefficient increment.
(2) Step –1 dB per coefficient increment.

Fig.6 Relation between APU coefficient index and gain.

7.16 Decoding control signals

The decoding is performed by 3 signals as shown in Table 6.

Table 6 Signals for decoding control

SIGNAL	DIRECTION	FUNCTION(1)
RESET		reset SAA2501 to default state
STOP	input	stop decoding
URDA	input	unreliable input data; interrupt decoding

The master reset signal RESET forces the SAA2501 into its default state when HIGH. RESET must stay HIGH during at least 24 MCLKIN periods if MCLKIN has frequency of 24 MHz (i.e. MCLK24 = 1) or 12 MCLKIN periods if MCLKIN has a frequency of 12 MHz (MCLK24 = 0). At a reset, the SAA2501 synchronization to the input bitstream is lost, the sub-band filter and baseband audio output signals are muted, and the SAA2501 settings are initialized.

The decoding can be stopped by making input signal STOP HIGH. Stopping the decoding forces the SAA2501 to end decoding of input data, yet feeding zeroed sub-band samples to the synthesis sub-band filter bank to create a soft muting. When using the master input, input requesting is also stopped. CDMWS stays in its current state while STOP is asserted. The SAA2501 assumes the input synchronization to be lost when the decoding is stopped, thus causing re-synchronization when STOP is de-activated again. Then the SAA2501 mutes, meanwhile searching for a frame sync pattern or frame sync pulse (the synchronization mode is selected via the L3 control bus) at the input.

If synchronization is found, the SAA2501 starts producing output data. The maximum response time to the activation of signal STOP is half a sample period; the re-synchronization time after STOP going LOW again differs in various situations.

An ‘unreliable data’ indication can be given to the SAA2501 by making signal URDA HIGH. URDA, like STOP, mutes the sub-band signals and forces the SAA2501 out of synchronization. However, in contrast to STOP, master input data requesting continues at the bit rate that was decoded before URDA became active. The maximum response time to URDA is half a sample period.

7.17 Coded data interfaces

The SAA2501 contains:

- A coded data master input interface
- A coded data slave input interface (designed for EU147 format).

7.17.1 The coded data master input interface

When using the master input, the SAA2501 requests for input data. With the master input, the coded input data may not use the ISO/MPEG free format bit rate or be in EU147 format. The coded data master input interface consists of 4 signals (see Fig.7).

Table 7 Signals of coded data master input interface

SIGNAL	DIRECTION	FUNCTION
CDM	input	ISO/MPEG coded input data (master input)
CDMEF	input	coded data (master input) error flag
CDMCL	output	coded data (master input) bit clock
CDMWS	output	coded data (master input) word select

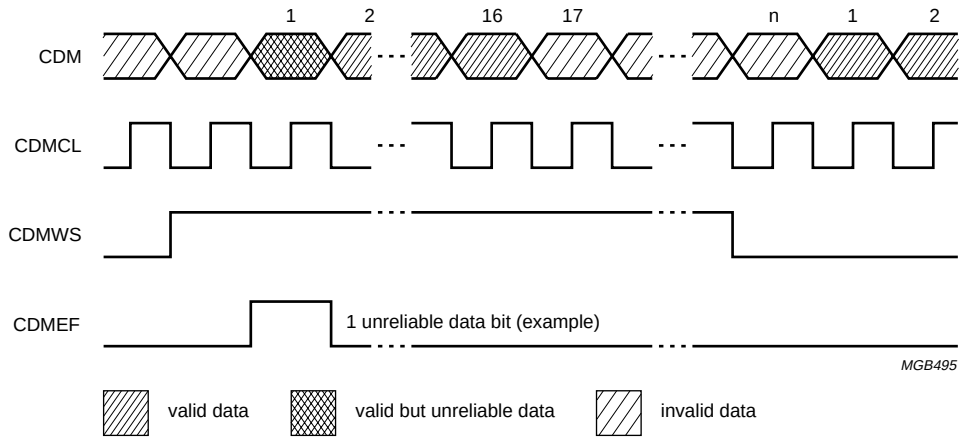


Fig.7 Input data serial transfer format (master input).

Data clock CDMCL is being output, having a fixed frequency of 768 kHz. Signal CDM carries the coded data in bursts of 16 valid bits. Coded data input frames may only start either at the first or at the ninth bit of a 16 bit valid data burst (i.e. only at a byte boundary). The value of word select signal CDMWS is changed every time new input data is needed: one CDMCL period after each transition in CDMWS, 16 bits of valid data are read serially. Assume N is the number of CDMCL periods between two transitions of CDMWS, and R is the number of CDMCL periods to obtain the effective bit rate E (in kbits/s) at a transferring data rate of 768 kbits/s, i.e. $R = \frac{16 \times 768}{E}$. The SAA2501 keeps N close to R, but N can vary plus or minus two: $N \in \{round(R)-2,...,round(R)+2\}$.

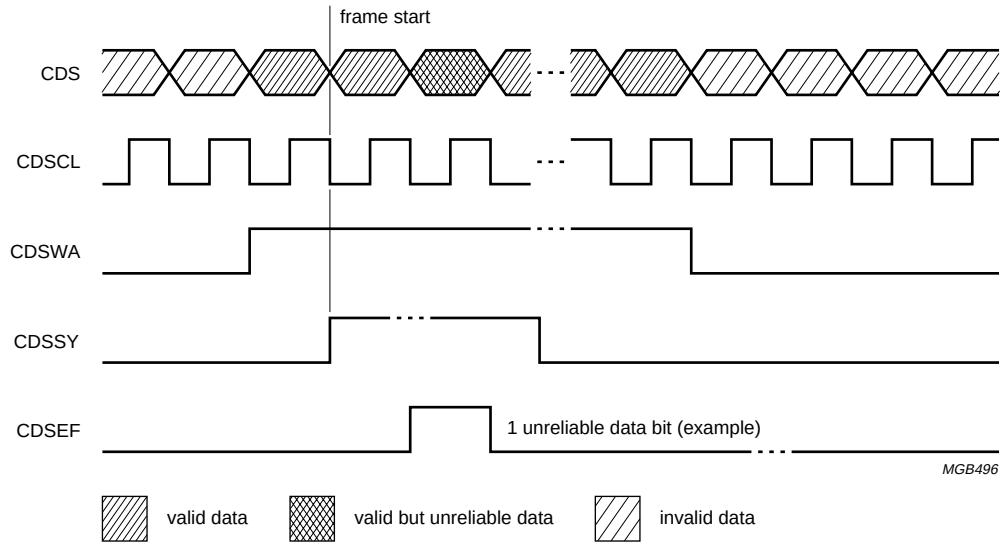
Error flag CDMEF is used to indicate input data insecurities (e.g. due to erratic channel behaviour). In Fig.7, an example with one unreliable bit is shown. The value of CDMEF may vary for each valid data bit, but is combined by the SAA2501 for every group of 8 input bits.

7.17.2 The coded data slave input interface

The coded data slave input interface signals are shown in Fig.8. The coded data master input interface consists of 5 signals (see Table 8).

Table 8 Signals of coded data slave input interface

SIGNAL	DIRECTION	FUNCTION
CDS	input	ISO/MPEG or EU147 coded input data (slave input)
CDSEF	input	coded data (slave input) error flag
CDSCL	input	coded data (slave input) bit clock
CDSWA	input	coded data (slave input) burst window signal
CDSSY	input	coded data (slave input) frame sync

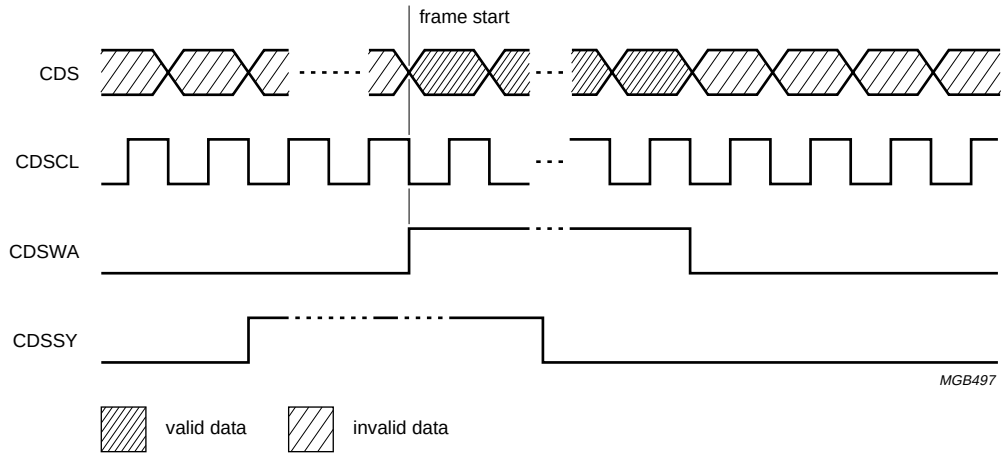


CDSSY indicates frame start during valid data.

Fig.8 Input data serial transfer format (slave input).

CDS is the SAA2501 input data bitstream. Data clock CDSCL must have a frequency equal to or higher than the bit rate. The maximum CDSCL frequency is 768 kHz. Error flag CDSEF is handled in the same way as CDMEF is handled for the master input (in Fig.8, one unreliable data bit is shown as an example). The value of CDSEF is neglected for those bits where CDSWA is LOW. Window signal CDSWA being HIGH indicates valid data; in this way, burst input data is allowed. The constraints for the ability to use 'burst signals' are explained later in this Section 7.17.2. Frame sync signal CDSSY indicates the start of each input data frame. CDSSY is synchronous with CDSCL. CDSSY may be present or not: as described later in this Section 7.17.2. The first valid CDS bit after a leading edge of CDSSY is interpreted to be the first frame bit.

The minimum time for CDSSY to stay HIGH is one CDSCL period; the maximum HIGH period is constrained by the requirement that CDSSY must be LOW at least during one CDSCL period per frame (a leading edge, i.e. a frame start indication, must be present every frame). Leading edges of CDSSY can occur while CDSWA is HIGH, as in Fig.8. Alternatively, a situation as shown in Fig.9 is also allowed, where CDSSY has a leading edge while CDSWA is LOW, i.e. during invalid data. The first CDS bit after CDSWA going HIGH is now interpreted to be the first frame bit.



CDSSY indicates frame start at next valid data.

Fig.9 Input data serial transfer format (slave input).

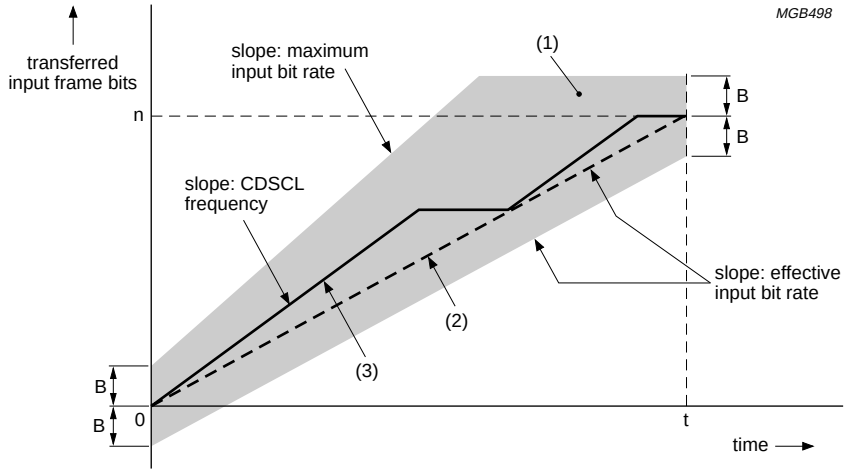
Whether frame sync signal CDSSY is present or not must be selected with L3 settings flags MSEL1 and MSEL0 (see Section 7.20.7). With respect to the presence of CDSSY, two situations can be distinguished:

1. For EU147 coded input data CDSSY is mandatory.
2. For ISO/MPEG input data if CDSSY is supplied, CDSWA may change each CDSCL period.
3. If CDSSY is not supplied, CDSCL must have a frequency higher than the bit rate (i.e. CDSWA cannot be continuously HIGH), and CDSWA HIGH periods may have only lengths of a multiple of 8 CDSCL periods: data is input in byte bursts. Furthermore, these bursts must be byte aligned with the frame bounds: frames are only allowed to start at the 1st, 9th, 17th etc. bit in a valid data burst. For applications where data is input in bursts of exactly one frame, and where CDSCL has a higher frequency than the bit rate, CDSWA and CDSSY may be interconnected.

7.17.3 Slave input transfer speed of first frame

Both the average and the instantaneous speed at which data is transferred to the slave input interface are limited. The data transferring of the first ISO/MPEG or EU147 frame after starting to decode is shown in Fig.10.

It shows the transferring of n-frame bits in one frame between time 0 and t, where t corresponds to 384 sample periods (ISO/MPEG layer I input data) or 1152 sample periods (ISO/MPEG layer II input data). Buffer margin B equals 16 bytes (128 bits). In Fig.10 an effective transferring characteristic is drawn, representing any of the possible ISO/MPEG bit rates. However, input data may be transferred at a higher-than-effective speed (in other words: CDSCL may have a higher frequency than the effective bit rate) in periods during which CDSWA is HIGH, interleaved with invalid data periods where CDSWA is LOW. In the example of Fig.9 this is used to transfer the data of the frame in two bursts, as shown by the actual transferring characteristic. The actual transferring characteristic has a slope equal to the CDSCL frequency while CDSWA is HIGH, and is horizontal during the periods in which CDSWA is LOW (no bits are being transferred).



(1) The actual transferring characteristics of all frames are restricted to this area.
(2) Effective transferring characteristic (example).
(3) Actual transferring characteristic of the first frame (example).

Fig.10 Slave input data transferring for the first frame.

The shaded area in Fig.10 represents the restrictions to the actual transferring characteristic of all frames. The actual transferring characteristic may not undercut the effective transferring characteristic by more than B bits to avoid an input underflow. On the other hand, the actual transferring characteristic may not cross the shown upper limit of the shaded area to prevent an input buffer overflow. The slope of this upper limit is determined by the maximum effective input bit rate (depending on the input data format). Table 9 summarizes the slopes as determined by the bit rates supported by ISO/MPEG and EU147.

Table 9 Slopes determined by bit rates supported by ISO/MPEG and EU147

ISO/MPEG AND EU147 LAYER	EFFECTIVE INPUT BIT RATE (kbits/s)	TRANSFERRING UPPER LIMIT SLOPE (kbits/s)
ISO/MPEG layer I	±13.3[1] to ±448	448
ISO/MPEG layer II	3.5[1] to 384	384

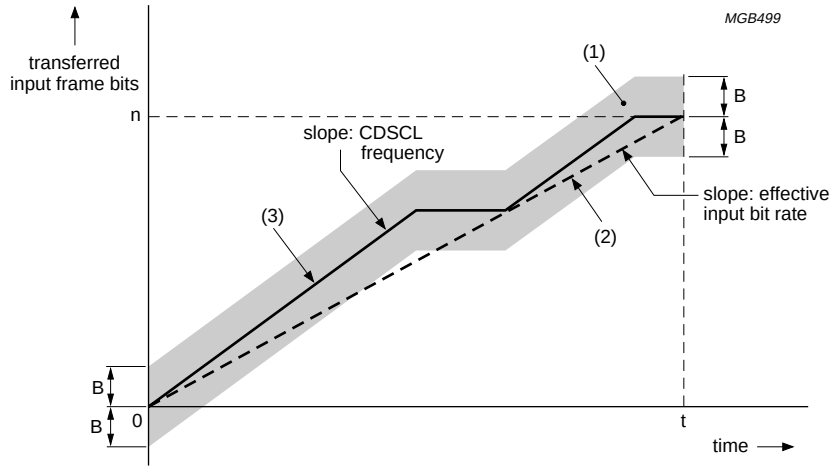
Note

1. Achieved using the free format option and the minimum amount of the side information that must be transmitted (this means using single channel mode, no CRC and 32 kHz sample rate).

7.17.4 Slave input transfer speed of subsequent frames

The SAA2501 starts decoding as soon as enough data of the first ISO/MPEG or EU147 input data frame has been received. Thus the start moment of decoding depends on the actual transferring characteristic of the first frame. Decoding start times of subsequent input data frames are also governed by this initial start time.

For this reason the transferring characteristic of all subsequent frames must approximate the characteristic of the first frame within the buffer margin ±B. For the example shown in Fig.10, subsequent frames must be transferred within the shaded area shown in Fig.11.



(1) The actual transferring characteristics of all subsequent frames are restricted to this area.
(2) Effective transferring characteristic (example).
(3) Actual transferring characteristic of the first frame (example).

Fig.11 Slave input data transferring for subsequent frames, referenced to the first frame.

Note that the actual transferring characteristics of all frames must also remain inside the shaded area of Fig.11.

7.18 The sub-band filter interface

As mentioned earlier, decoded signals in the sub-band domain (before synthesis filtering) are available externally for processing. The associated interface has an I^2S-like format (see Fig.12).

The filter data interface uses 6 signals as shown in Table 10.

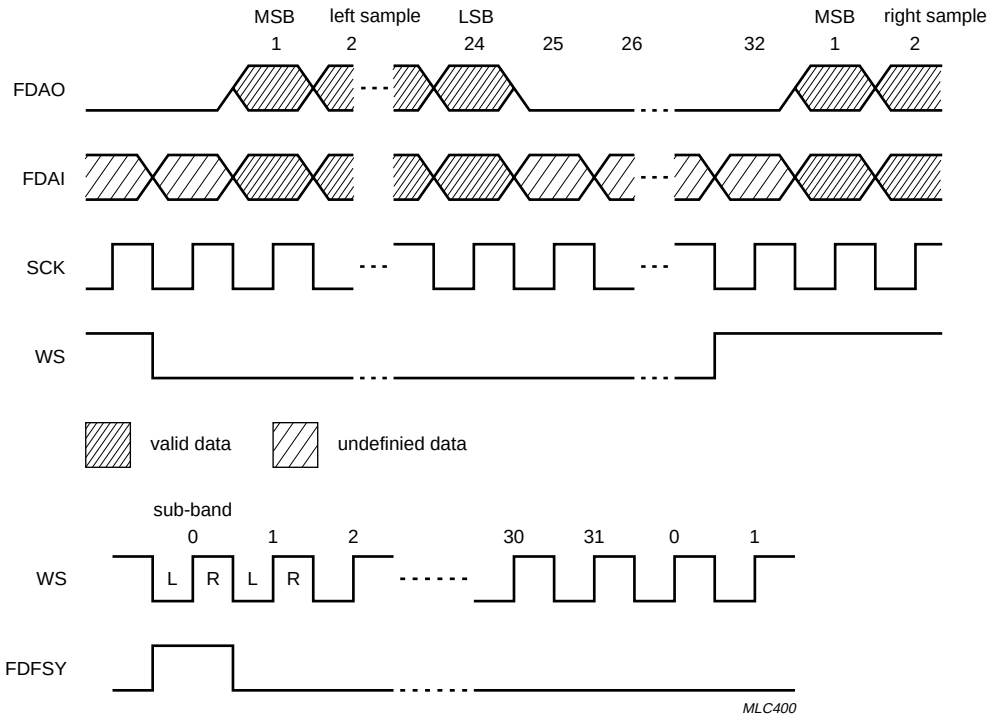


Fig.12 Filter data serial transfer format.

Table 10 Signals of filter data interface

SIGNAL	DIRECTION	FUNCTION
FDAO	output	filter data output
FDEF	output	filter data error flag
FDAI	input	filter data input (optionally processed)
SCK	output	filter data (output/input common) bit clock; I^2S clock output
WS	output	filter data (output/input common) word select; I^2S
FDFSY	output	filter data output frame synchronization

Two sub-band samples (one per channel) are transmitted per sample period with output FDAO. The transmission pattern of the samples S [sb, ch] (sb: sub-band index; ch: channel) is: S [0, L], S [0, R], S [1, L], S [1, R],..., S [31, R], S [0, L], S [0, R], etc. Word select signal WS indicates the channel of each sample (WS is also used for the baseband audio output interfacing).

The sub-band sample bit clock SCK has a frequency of 64 times the sample frequency. The sub-band samples are transmitted in 24 bit two's complement Pulse Code Modulation (PCM) form, MSB first. Thus, of the available 32 FDAO bits per sample per channel, only 24 are used.

The MSB of a sample follows one SCK period after each transition in WS. The 8 unused bits between individual samples in FDAO are zero (SCK is used for the baseband audio output interface as well). The optionally processed sub-band data signal is fed back as input FDAI in a similar format as FDAO, but now the 8 unused bits between individual samples are undefined; they are neglected by the SAA2501.

A leading edge in signal FDFSY indicates the start of each FDAO frame. The length of each FDFSY pulse is one sample period; FDFSY is HIGH during a S[0,L] and S[0,R]

pair. Signal FDEF being HIGH indicates muting of FDAO due to input data errors (see Fig.13).

FDEF can only change value at each FDFSY leading edge, i.e. after each 384 sample periods (ISO/MPEG layer I input data) or 1152 sample periods (ISO/MPEG layer II input data): only whole frames are marked to be correct or muted. As shown in detail in Fig.13, transitions of FDFSY and FDEF take place one SCK period before a trailing edge of WS.

The optionally processed sub-band data FDAI must be synchronous to SCK and WS. Furthermore, the sub-band index of the FDAI samples must be synchronized to FDFSY: a sub-band logic 0 sample pair must be input when FDFSY is HIGH (as shown in Fig.12). This means that the delay of the external processing is allowed to be any integer multiple of 32 sample periods. If no external processing is to be applied, FDAO must be input back directly to FDAI.

7.19 The baseband output interface

The decoded baseband audio data is output in an I^2S-like format (see Fig.14).

The output interfacing consists of 3 signals (see Table 11).

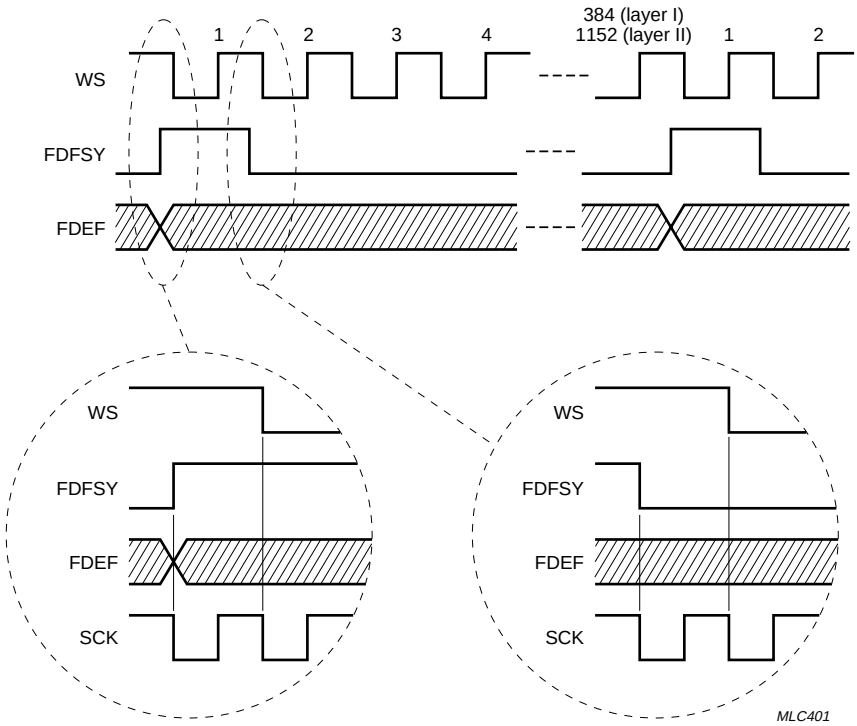


Fig.13 Filter data error flag (FDEF) timing.

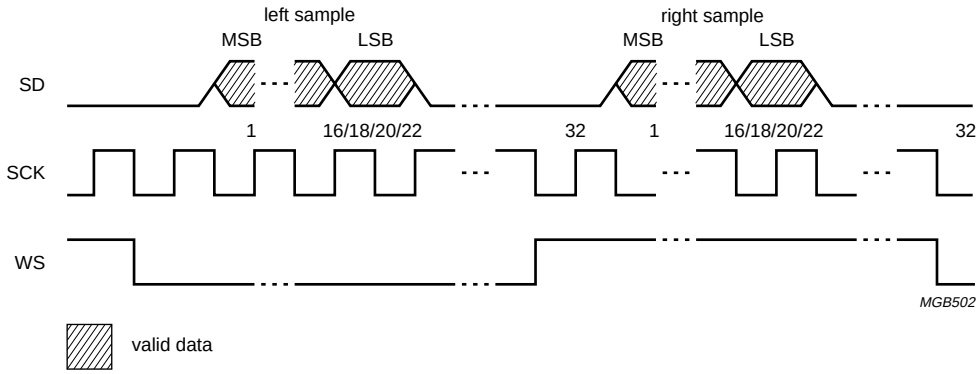


Fig.14 Baseband output data serial transfer format.

Table 11 Signals of output interfacing

SIGNAL	DIRECTION	FUNCTION
SD	output	baseband audio data
SCK	output	data clock
WS	output	word select

The frequency of clock SCK is 64 times the sample frequency (SCK is also used for the sub-band filter interface).

The signal SD is the serial baseband audio data, sample by sample (left/right interleaved; the left sample and the right immediately following it form one stereo pair). 32 bits are transferred per sample per channel. The samples are transmitted in two's complement, MSB first. The output samples are rounded to either 16, 18, 20 or 22 bit precision, selectable by the host with L3 control interface flags RND1 and RND0. The remainder of the 32 transferred bits per sample per channel are zero.

The word select signal WS indicates the channel of the output samples (LOW if left, HIGH if right); WS is used for the sub-band filter interface as well. If indicated in the coded input data, de-emphasis filtering is performed digitally on the output data, thus avoiding the need of analog de-emphasis filter circuitry.

7.20 The L3 control interface

The SAA2501 uses the L3 protocol with the associated bus as the control interface with an optional host microcontroller (see Chapter 8 for more information). In the programming sections a general transfer protocol outline is presented. In Section 8.2 several optional protocol enhancements are given, which on the one hand are less transparent from the applicant's point of view, but on the other hand increase the efficiency of the L3 interfacing.

7.20.1 L3 SIGNALS

The L3 protocol uses 3 signals (see Table 12).

Table 12 Signals of L3 protocol

SIGNAL	DIRECTION	FUNCTION
L3DATA	input/output	L3 interface serial data
L3CLK	input	L3 interface bit clock
L3MODE	input	L3 interface address/data select

The signals operate according to the L3 protocol description. After each device reset, the L3 interface of the SAA2501 must be initialised and as a consequence, the L3 interface cannot be used while the device reset signal is activated.

7.20.2 L3 TRANSFER TYPES

The L3 protocol enables the reading and writing of control, status and data. In the L3 protocol, the host first issues an 8 bit wide 'operational address' on L3DATA while keeping L3MODE LOW. All devices connected to the L3 bus read the operational address. Next, data transfers from or to the host are done while keeping L3MODE HIGH. The devices with an L3 operational address differing from the issued one must ignore these data transfers until the next operational address is issued. Only the device with an address equal to the issued operational address performs the transfer.

The SAA2501 has the L3 operational address as shown in Table 13.

Table 13 L3 operational address.

7	6	5	4	3	2	1	0
0	1	1	0	0	0	DOM1[1]	DOM0[1]

Note

1. The 'Data Operation Mode' bits DOM1 and DOM0 determine the mode in which the SAA2501 L3 interface will stay until the next time an L3 operational address is issued (see Table 14).

Table 14 DOM1 and DOM0 bits

DOM1	DOM0	TRANSFER TYPE
0	0	write item data
0	1	read item data
1	0	write control to SAA2501
1	1	read SAA2501 status

Control bytes can be written to the SAA2501.

Data is transferred to or from the SAA2501 in so-called data items. The items can be a readable or writeable type. A data item transfer is initiated by writing the corresponding control byte to the SAA2501 first. Next, the item data itself is transferred, always as an integer number of bytes.

The status of the SAA2501 can be read via L3. The SAA2501 status flag L3RDY must be monitored before transferring data item bytes to avoid transferring bytes faster than the L3 interface of the SAA2501 can handle.

7.20.3 L3 INTERFACE INITIALIZATION AT AN SAA2501 DEVICE RESET

Figure 15 shows the mandatory actions that must be taken for correct L3 interface start-up at a device reset.

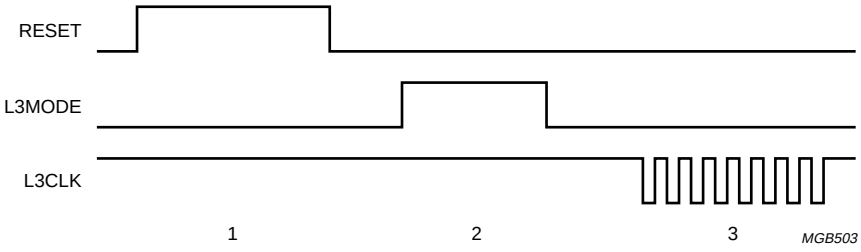


Fig.15 L3 interface initialization procedure.

The actions shown in Fig.15 are:

1. In order for the SAA2501 to keep L3DATA in 3-state, L3MODE must be kept LOW during the whole period that reset signal at pin RESET is asserted; meanwhile, no transfers can be performed (L3CLK stays HIGH).
2. For a proper initialization of the L3 interface logic of the SAA2501, it is mandatory to make L3MODE HIGH and LOW again after the device reset has been de-activated. This must be done before any L3 transfer, even to or from other devices than the SAA2501, is performed. Figure 14 shows that L3CLK stays HIGH during this step.
3. Now the first transfer can be performed on the L3 bus. This transfer must be a operational address (indicated in Fig.14 by L3MODE = 0), addressing any of the devices connected to the L3 bus. The first transfer to the SAA2501 itself must always be either the writing of a control word or the reading of the SAA2501 status; the first transfer may never be a data item byte transfer.

Remark: any deviation from these steps may result in illegal L3 protocol behaviour of the SAA2501, even with the possibility of disturbing transfers to other devices connected to the L3 bus.

7.20.4 L3 INTERFACE CONTROL

The control of the SAA2501 L3 interface is performed with one-byte control words. Status polling is not necessary before writing control bytes. After writing the SAA2501 'write control' operational address, one or more control bytes may be written. Each written control byte overrules the previously sent control byte.

Table 15 L3 control

7	6	5	4	3	2	1	0
CTRL7	CTRL6	CTRL5	CTRL4	CTRL3	CTRL2	CTRL1	CTRL0

The definitions of the control bytes (CTRL7 to CTRL0) are given in Table 16.

Table 16 Explanation of control bytes

CTRL7 TO CTRL0	DEFINITION	TYPE[1]
00000000	read/write SAA2501 settings item	I
00000001	read decoded frame header item	I
00000010	read used frame header item	I
00000011	read error report item	I
00000100	reserved	I
00000101	read Ancillary Data item	I
00000110	write APU coefficients item	I
00000111	continue previous transfer	C
00001000 to 11111111	reserved	–

Note

1. Control bytes of type I initiate the transfer of a data item. The control byte of type C may be used after interrupting a transfer, in order to write APU coefficients, to return to the interrupted transfer.

7.20.5 SAA2501 STATUS

The host can check the status of the SAA2501 by reading the one-byte status word. After writing the SAA2501 'read status' operational address, the status byte may be read an arbitrary number of times. If status is read more than once, it is updated by the SAA2501 between the individual readings. The status flags of the SAA2501 have the definition as shown in Table 17.

Table 17 Status flag definitions

7	6	5	4	3	2	1	0
DST2(1)	DST1(1)	DST0(1)	undefined	undefined	undefined	INSYNC(2)(3)	L3RDY(4)

Notes

1. By interpreting DST2 to DST0, the host can synchronize to the input frame frequency, and also determine at which moment which L3 data item is available to be read. The value of DST2 to DST0 is only valid if flag INSYNC is set.
   a) DST2 is a modulo 2 frame counter, i.e. DST2 inverts at the moment the decoding of a new frame is started. DST2 enables to host to sample the decoding subprocess DST1 to DST0 less frequently, meanwhile enabling the host to see if it missed a state.
   b) DST1 and DST0 values are explained in Table 18.
2. INSYNC is synchronization indication:
   a) INSYNC = 0; the SAA2501 is not synchronized to the input data.
   b) INSYNC = 1; the SAA2501 is synchronized to the input data.
3. As indicated in Section 7.20.8, some of the readable data item bits only have significance if INSYNC = 1.
4. L3RDY is L3 interface ready indication:
   a) L3RDY = 0; the L3 interface cannot perform a new item data transfer yet.
   b) L3RDY = 1; the L3 interface is ready for the next item data transfer.

   After a device reset, L3RDY is cleared and will only become set after writing the first L3 control byte to the SAA2501. The value of L3RDY can be tested by polling signal L3DATA instead of transferring the whole status byte.

Table 18 Status bytes DST1 and DST0

DST1	DST0	FUNCTION
0	0	subprocess 0; reading Ancillary Data or decoding header
0	1	subprocess 1; decoding bit allocation or scale factor select information
1	0	subprocess 2; decoding scale factors
1	1	subprocess 3; decoding samples

The DST1 and DST0 values in general do not have a determined duration. However, subprocess 3 takes at least $\frac{1}{2}$ a frame period when ISO/MPEG layer I data is decoded, and $\frac{5}{6}$ of a frame period when ISO/MPEG layer II data is decoded. Table 19 indicates the validity of the SAA2501 readable data items with respect to the decoding subprocess. Reading of a data item in a period when it is not valid renders undefined data.

Table 19 Validity of SAA2501 readable data items with respect to the decoding subprocess (notes 1 and 2)

<table>
<tr><th colspan="4">SAA2501 IS DECODING FRAME n</th><th colspan="4">SAA2501 IS DECODING FRAME n + 1</th></tr>
<tr><th colspan="4">DST2 = 0; SUBPROCESS</th><th colspan="4">DST2 = 1; SUBPROCESS</th></tr>
<tr><th>0</th><th>1</th><th>2</th><th>3</th><th>0</th><th>1</th><th>2</th><th>3</th></tr>
<tr><td rowspan="2">not valid</td><td colspan="3">Ancillary Data item (frame n – 1)</td><td rowspan="2">not valid</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td colspan="3">frame header items (frame n)</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>–</td><td rowspan="2">not valid</td><td colspan="2">error report: BALOK (frame n)</td><td rowspan="2">not valid</td><td>–</td><td>–</td></tr>
<tr><td>–</td><td>not valid</td><td>error report: DECFM (frame n)</td><td>not valid</td><td>–</td></tr>
</table>

Notes

1. The Table shows following:
   a) The received Ancillary Data that was multiplexed in frame n–1 becomes valid after subprocess 0 of frame n, and may be read during subprocesses 1, 2 and 3 of frame n.
   b) The decoded and used frame headers for frame n become valid after subprocess 0 of frame n, and may be read during subprocesses 1, 2 and 3 of frame n.
   c) Flag BALOK for frame n in the error report item becomes valid after subprocess 1 of frame n, and may be read during subprocesses 2 and 3 of frame n and subprocess 0 of frame n+1.
   d) Flag DECFM for frame n in the error report item becomes valid after subprocess 2 of frame n, and may be read during subprocesses 3 of frame n and 0 of frame n+1.
2. Note that during subprocess 3 all data items can be read.

7.20.6 DATA ITEMS

Data can be transferred to or from the SAA2501 in data items. This section describes the general protocol to accomplish item data transfer, followed by the individual SAA2501 data items. Optional enhancements on the general protocol are described in Chapter 8 Section 8.2.

7.20.6.1 General data items

The data items of the SAA2501 are transferred (i.e. read or written, depending on whether the data item is of readable or writeable type) in bytes. A data item transfer is initiated by writing the corresponding type I control byte (see Section 7.20.4) to the SAA2501. The transfer of every subsequent item data byte must be preceded by reading the status until status flag L3RDY (see Section 7.20.5) is HIGH.

L3RDY may be tested alternatively by polling L3DATA, avoiding the need to transfer the whole status byte. Status polling is not required while transferring the APU coefficients item. Table 20 shows an example of how bytes ‘DDDDDDDD’ of a 2 byte data item, with the corresponding control byte ‘CCCCCCCC’, can be read. The writing of item data bytes occurs in a similar way.

Table 20 Example of a 2 byte data item

L3DATA(1)	TRANSFER SOURCE	L3MODE	EXPLANATION
01100010	host	0	indicates ‘write control’ transfer
CCCCCCCC	host	1	write transfer initiating (type I) control byte
01100011	host	0	indicates ‘read status’ transfer
SSSSSSSS	SAA2501	1	read status (repeat step 4 until L3RDY = 1)
01100001	host	0	indicates ‘read item data’ transfer
DDDDDDDD	SAA2501	1	read first item data byte
01100011	host	0	indicates ‘read status’ transfer
SSSSSSSS	SAA2501	1	read status (repeat step 8 until L3RDY = 1)
01100001	host	0	indicates ‘read item data’ transfer
DDDDDDDD	SAA2501	1	read second item data byte

Note

1. Explanation of bytes:
   a) CCCCCCCC = control byte.
   b) SSSSSSSS = status byte.
   c) DDDDDDDD = data byte.

Each data item has its own length in bytes. It is allowed to transfer less bytes than the data item length, skipping the last one or more bytes (it is even allowed to transfer no bytes at all). It is not allowed to transfer more bytes than the item length. This restriction does not hold for the APU coefficient item. After writing all APU coefficients (i.e. after writing all APU coefficient item bytes), they may be rewritten by continuing writing bytes to the APU coefficient item. Writing more than the specified number of bytes to a writeable data item or writing bytes to a read-only data item may cause the SAA2501 to malfunction. The reading of a write-only data item yields irrelevant data.

7.20.7 SAA2501 SETTINGS ITEM

The SAA2501 is configured with the SAA2501 settings. The initial value of the SAA2501 settings after reset is all zeros.

Table 21 SAA2501 settings item; 1 byte (read/write)

7	6	5	4	3	2	1	0
MSEL1(1)	MSEL0(1)	CRCACT(2)	MCKDIS(3)	FCKENA(4)	SELCH2(5)	RND1(6)	RND0(6)

Notes

1. MSEL1 and MSEL0; these bits select the used input interface, the input data format and the input synchronization type (see Table 22).
2. CRCACT; automatic/forced CRC activity:
   a) CRCACT = 0; the SAA2501 uses the protection bit in the ISO/MPEG frame header to determine the presence of the CRC.
   b) CRCACT = 1; the SAA2501 assumes the CRC always to be present. The protection bit in the used ISO/MPEG frame header is forced to 0.
3. MCKDIS; buffered master clock MCLK disabling:
   a) MCKDIS = 0; enable MCLK.
   b) MCKDIS = 1; disable (3-state) MCLK.
4. FCKENA; buffered $256f_s$ or $384f_s$ output signal FSCLK enabling:
   a) FCKENA = 0; disable (3-sate) FSCLK.
   b) FCKENA = 1; enable FSCLK.
5. SELCH2; with dual channel mode input data (with other modes of input data ‘don’t care’:
   a) SELCH2 = 0; select channel I.
   b) SELCH2 = 1; select channel II.
6. RND1 and RND0; these bits select the rounding of the baseband audio output samples (see Table 23).

Table 22 MSEL1 and MSEL0

MSEL1	MSEL0	USED INPUT INTERFACE	INPUT SYNCHRONIZATION
0	0	master	to ISO/MPEG synchronization pattern
0	1	EU147	to synchronization signal CDSSY
1	0	slave	to ISO/MPEG synchronization pattern
1	1	slave	to synchronization signal CDSSY

Table 23 RND1 and RND0

RND1	RND0	OUTPUT SAMPLE ROUNDING LENGTH
0	0	16 bits
0	1	18 bits
1	0	20 bits
1	1	22 bits

7.20.8 INPUT DATA FRAME HEADER ITEMS

Information about the input data, derived by the SAA2501 from the input data frame headers, may be read from the frame header items. Both the frame header bytes decoded from the input bitstream and the header bytes used for the actual decoding may be read.

The decoded frame header item is valid independent of the value of status flag INSYNC, it e.g. shows the decoded headers while the SAA2501 is in the process of synchronizing.

The used frame header item is only valid if status flag INSYNC is set. The used header bytes are derived by the SAA2501 from the decoded header bytes by overruling NOPR to 0 if settings bit CRCACT = 1, and overruling detected errors.

Table 24 Decoded input data frame header item; 3 bytes (read-only)

SUBSEQUENT BYTES	7	6	5	4	3	2	1	0
Decoded header byte 1	SY3[1]	SY2[1]	SY1[1]	SY0[1]	ID[2]	LAY1[3]	LAY0[4]	NOPR[5]
Decoded header byte 2	BR3[6]	BR2[6]	BR1[6]	BR0[6]	FS1[7]	FS0[7]	undefined	undefined
Decoded header byte 3	MOD1[8]	MOD0[8]	MODX1[9]	MODX0[9]	COPR[10]	ORIG[11]	EMPH1[12]	EMPH0[12]

Table 25 Used input data frame header item; 3 bytes (read-only)

SUBSEQUENT BYTES	7	6	5	4	3	2	1	0
Used header byte 1	1	1	1	1	1	1	LAY0[4]	NOPR[5]
Used header byte 2	BR3[6]	BR2[6]	BR1[6]	BR0[6]	FS1[7]	FS0[7]	undefined	undefined
Used header byte 3	MOD1[8]	MOD0[8]	MODX1[9]	MODX0[9]	COPR[10]	ORIG[11]	EMPH1[12]	EMPH0[12]

Notes to “Table 24” and “Table 25”

1. SY3 to SY0; last 4 bits of the synchronization word. For ISO/MPEG only; undefined for EU147 input data.
2. ID; algorithm identification. For ISO/MPEG only; undefined for EU147 input data.
3. LAY1; layer Most Significant Bit (MSB). For ISO/MPEG only; undefined for EU147 input data.
4. LAY0; layer Least Significant Bit (LSB). When decoding EU147 input data these bits are undefined in the decoded header byte and equal 0 in the used header byte.
5. NOPR; CRC on header, bit allocation and scale factor select information activity flag. When decoding EU147 input data these bits are undefined in the decoded header byte and equal 0 in the used header byte.
6. BR3 to BR0; bit rate index.
7. FS1 and FS0; sample rate index.
8. MOD1 and MOD0; mode.
9. MODX1 and MODX0; mode extension.
10. COPR; copyright flag.
11. ORIG; original or home copy flag.
12. EMPH1 and EMPH0; audio de-emphasis, these bits are only meant to monitor the current de-emphasis mode; the corresponding de-emphasis is performed by the SAA2501 automatically before the baseband audio signal is output.

7.20.9 Error report item

The validity of bit allocation plus scale factor select information and the result of the scale factor CRCs (the latter only when decoding EU147 input data) may be read from the error report item. The error report item is only valid if status flag INSYNC is set.

Table 26 Error report item; 1 byte (read-only)

SUBSEQUENT BYTES	7	6	5	4	3	2	1	0
Error report	BALOK(1)	DECFM(2)	undefined	undefined	SF3OK(3)	SF2OK(3)	SF1OK(3)	SF0OK(3)

Notes

1. BALOK; bit allocation and scale factor select information validity indication:
   a) BALOK = 0; bit allocation or scale factor select information are incorrect, or the CRC (if active) over header, bit allocation and scale factor select information fail.
   b) BALOK = 1; bit allocation or scale factor select information are correct, and the CRC (if active) over header, bit allocation and scale factor select information passes.
2. DECFM; frame skipping/decoding indication:
   a) DECFM = 0; the current input data frame is skipped, and the corresponding baseband audio output frame is muted due to input data errors or inconsistencies. However, synchronization to the input data is maintained.
   b) DECFM = 1; the current frame is decoded normally.
3. SFnOK is invalid when decoding ISO/MPEG input data. When decoding EU147 input data:
   a) SFnOK = 0; then one or more scale factors have been concealed in sub-band block (n).
   b) SFnOK = 1; no scale factors in sub-band block (n) are concealed (i.e. the error checking has passed).

   Blocks 0 to 3 are explained in Table 27.

Table 27 Content of blocks 0 to 3

BLOCK	SUB-BANDS
0	0 to 3
1	4 to 7
2	8 to 15
3	16 to 31

7.20.10 Audio service synchronized data item

When decoding EU147 input data, the Audio Service Synchronized Data (ASSD), which is contained in each frame, may be read. The subsequent ASSD bytes are read in reverse order with respect to the input bitstream; the first ASSD item byte is the last byte in the input bitstream. The ASSD item is only valid when the status flag INSYNC is set.

Table 28 ASSD item; 2 bytes (read-only)

SUBSEQUENT BYTES	7	6	5	4	3	2	1	0
ASSD bytes 1 and 2	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

The ASSD item and the (extended) Program Associated Data [(X)PAD] item (see Section 7.20.11) may be read together as a single item.

7.20.11 Ancillary Data/XPAD item

The last 54 bytes of each ISO/MPEG frame, which may carry Ancillary Data (AD), are buffered by the SAA2501 to be read by the host. The subsequent Ancillary Data bytes are read in reversed order with respect to their order in the input data bitstream. The first item data byte is the last frame byte in the input bitstream. The Ancillary Data item is refilled at every frame. The host must either know or determine itself how many of the Ancillary Data bytes are valid per frame. The Ancillary Data item only has significance if status flag INSYNC is set.

Table 29 Ancillary Data item; 54 bytes (read-only)

SUBSEQUENT BYTES	7	6	5	4	3	2	1	0
AD byte 1 to AD byte 54	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Likewise, when EU147 input data is being decoded, the PAD and XPAD bytes contained in each frame may be read, with the 2 PAD bytes first, followed by a maximum of 52 XPAD bytes. The subsequent PAD and XPAD bytes are read in reversed order with respect to their order in the input data bitstream. The first item data byte is the last PAD byte in the input bitstream. The host must determine itself how many of the XPAD bytes are valid per frame by interpretation on the PAD. The (X)PAD item only contains significant data if status flag INSYNC is set.

Table 30 (X)PAD item; 54 bytes (read-only)

SUBSEQUENT BYTES	7	6	5	4	3	2	1	0
PAD byte 1	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PAD byte 2	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
XPAD bytes 1 to 52	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

7.20.12 APU coefficients item

The APU coefficients are set by writing their 8 bit indices to the 4-byte APU coefficient item. Only the 7 LSBs are valid. The MSB must be zero. At a device reset, indices LL and RR are set to 00000000 (‘no attenuation’) and indices LR and RL to 01111111 (infinite attenuation; no crosstalk).

Table 31 APU coefficients item; 4 bytes (write-only); see note 1

SUBSEQUENT BYTES	7	6	5	4	3	2	1	0
APU coefficient LL	0	LL.6	LL.5	LL.4	LL.3	LL.2	LL.1	LL.0
APU coefficient LR	0	LR.6	LR.5	LR.4	LR.3	LR.2	LR.1	LR.0
APU coefficient RL	0	RL.6	RL.5	RL.4	RL.3	RL.2	RL.1	RL.0
APU coefficient RR	0	RR.6	RR.5	RR.4	RR.3	RR.2	RR.1	RR.0

Note

1. Multiple options are supplied by the SAA2501 to increase the timing accuracy of the APU coefficient writing (see Section 8.2).

7.20.13 Speed limitations of the L3 interface

When reading the status of, or writing control bytes to the SAA2501, no status polling is necessary, so the speed of these transfers is only limited by the maximum frequency of signal L3CLK and the timing constraints of the L3 protocol.

When reading or writing data item bytes, status polling is necessary. In addition to the speed limitation this poses, the application must take precautions that individual data item bytes are transferred at an interval of at least 200 µs.

Neither the status polling nor a minimum interval between transfers is required when transferring the APU coefficient item.

7.20.14 Default item data values after reset

At a device reset, the L3 interface initialization procedure must be followed. All writeable data items are pre-loaded with a defined default value after the device reset signal has been de-activated. These default values are summarized in Table 32.

Table 32 SAA2501 settings item; default value after device reset (notes 1 to 6)

SUBSEQUENT BYTES	7	6	5	4	3	2	1	0
SAA2501 settings	MSEL1	MSEL0	CRCACT	MCKDIS	FCKENA	SELCH2	RND1	RND0
Value	0	0	0	0	0	0	0	0

Notes

1. MSEL1 = 0 and MSEL0 = 0; the master input is selected. The SAA2501 synchronizes to the ISO/MPEG synchronization pattern.
2. CRCACT = 0; the SAA2501 uses the protection bit in the ISO/MPEG frame header to determine if the CRC is active.
3. MCKDIS = 0; the buffered master clock output MCLK is enabled.
4. FCKENA = 0; the buffered $256f_s$ or $384f_s$ clock output is disabled.
5. SELCH2 = 0; when decoding input data with dual channel mode, channel I is output on both baseband audio output channels.
6. RND1 = 0 and RND0 = 0; the baseband audio output signals are rounded to 16 bit.

Table 33 APU coefficients item; default values after device reset

SUBSEQUENT BYTES	7	6	5	4	3	2	1	0
APU coefficient LL(1)	0	LL.6 = 0	LL.5 = 0	LL.4 = 0	LL.3 = 0	LL.2 = 0	LL.1 = 0	LL.0 = 0
APU coefficient LR(2)	0	LR.6 = 1	LR.5 = 1	LR.4 = 1	LR.3 = 1	LR.2 = 1	LR.1 = 1	LR.0 = 1
APU coefficient RL(3)	0	RL.6 = 1	RL.5 = 1	RL.4 = 1	RL.3 = 1	RL.2 = 1	RL.1 = 1	RL.0 = 1
APU coefficient RR(4)	0	RR.6 = 0	RR.5 = 0	RR.4 = 0	RR.3 = 0	RR.2 = 0	RR.1 = 0	RR.0 = 0

Notes

1. LL = 00000000; no attenuation in the left-to-left APU path.
2. LR = 01111111; infinite attenuation in the left-to-right APU path.
3. RL = 01111111; infinite attenuation in the right-to-left APU path.
4. RR = 00000000; no attenuation in the right-to-right APU path.

8 APPENDIX

8.1 Preliminary specification 3-line ‘L3’ interface

8.1.1 INTRODUCTION

The main purpose of the new interface definition is to define a protocol that allows for the transfer of control information and operational details between a microcontroller and a number of slave devices, at a rate that exceeds other common interfaces, but with a sufficient low complexity for application in consumer products. It should be clearly noted that the current interface definition is intended for use in a single apparatus, preferably restricted to a single printed circuit-board.

The new interface requires 3 signal lines (apart from a return ‘ground’) between the microcontroller and the slave devices (from this the name ‘L3’ is derived). These 3-lines are common to all ICs connected to the bus: L3MODE, L3DATA and L3CLK. L3MODE and L3CLK are always driven by the microcontroller, L3DATA is bidirectional:

Table 34 The 3-lines common to all ICs; L3MODE, L3CLK and L3DATA

SIGNAL	MICROCONTROLLER	SLAVE DEVICE
L3MODE(1)	output	input
L3CLK(2)	output	input
L3DATA(3)	output/input	input/output

Notes

1. L3MODE is used for the identification of the operation mode.
2. L3CLK is the bit clock to which the information transfer will be synchronized.
3. L3DATA will carry the information to be transferred.

All slave devices in the system can be addressed using a 6-bit address. This allows for up to 63 different slave devices, as the all ‘0’ address is reserved for special purposes. In addition it is possible to extend the number of addressable devices using ‘extended addressing’.

During operation 2 modes can be identified:

1. Addressing mode (AM).

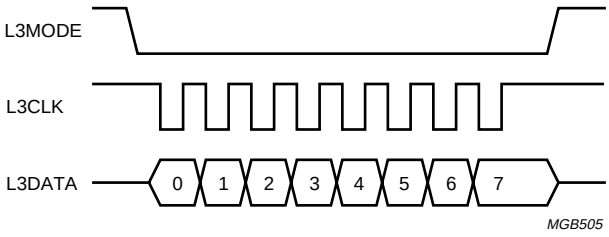
   During addressing mode a single byte is sent by the microcontroller. This byte consists of 2 data operation mode (DOM) bits and 6 operational address (OA) bits. Each of the slave devices evaluates the operational address. Only the device that has been issued the same operational address will become active during the following data mode. The operation to be executed during the data mode is indicated by the two data operation mode bits.

2. Data mode (DM).

   During data mode information is transferred between microcontroller and slave device. The transfer direction may be from microcontroller to slave (‘write’) or from slave to microcontroller (‘read’). However, during one data mode the transfer direction cannot change.

8.1.1.1 Addressing mode

In order to start an addressing mode the microcontroller will make the L3MODE line LOW. The L3CLK line is put to the LOW state 8 times and the DATA line will carry 8 bits. The addressing mode is ended by making the L3MODE line HIGH.



The meaning of the bits on L3DATA.

Bit 0 and bit 1; these are the data operation mode (DOM) bits that indicate the nature of the following data transfer. Each slave device may have its own allocation of operation modes to the 4 possible codes of these bits. For correct information about the operation the device will perform, refer to the descriptions of the individual ICs. For new designs the preferred allocations are given in Table 35.

Bit 2 to bit 7; these bits act as 6 bit (special function) operational IC address, with bit 7 as MSB and bit 2 as LSB. Bit 7 to bit 5 act as system identification and bit 4 to bit 2 as identification of the device within the system.

Fig.16 Addressing mode.

Table 35 Preferred allocations

DOM1	DOM0	FUNCTION	REMARKS
0	0	data from microcontroller to SAA2501	general purpose data transfer
0	1	data from SAA2501 to microcontroller	general purpose data transfer
1	0	control from microcontroller to SAA2501	e.g. register selection for data transfer
1	1	status from SAA2501 to microcontroller	short device status message

8.1.1.2 Special function operational address

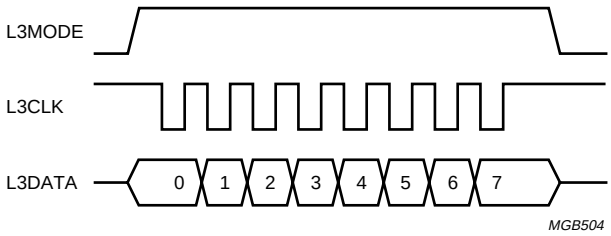


Fig.17 Data transfer mode.

Operational address 000000 (bit 2 to bit 7) is the special function address, and is used for the L3 device reset, as well as for the declaration and invalidation of the extended addressing. Both will be explained in Sections 8.1.2 and 8.1.3.

8.1.1.3 Data mode

In the data mode (see Fig.17) the microcontroller sends or receives information to or from the selected device. During data transfer the L3MODE line is HIGH. The L3CLK line is lowered 8 times during which the L3DATA line carries 8 bits. The information is presented LSB first and remains stable during the LOW phase of the L3CLK signal.

The preferred basic data transfer unit is an 8 bit byte. Some implementations that are modifications of earlier circuits with 16 bit registers may use a basic unit of 16 bits, transferred as 2 bytes, with the most significant byte presented first. No other basic data transfer unit is allowed.

8.1.1.4 Halt mode

In between units the L3MODE line will be driven LOW by the microcontroller to indicate the completion of a basic unit transfer. This is called ‘halt mode’ (HM). During halt mode the L3CLK line remains HIGH (to distinguish it from an addressing mode). The halt mode allows an implementation of an interface module without a bit counter. However, an implementation using a bit counter in the interface module may allow for the L3MODE line to be kept HIGH in between units (not using the halt mode).

This implementation must also operate correctly if the halt mode is used. The documentation of the device will have to indicate clearly whether or not the ‘halt mode’ is necessary for correct operation of the interface.

8.1.2 Device interface reset

If the microcontroller sends an operational address ‘000000’ with DOM1 and DOM0 also equal to ‘0’ this indicates that none of the L3 interface devices is allowed to communicate with the microcontroller during the following data mode. This enables a different application of the L3CLK and L3DATA lines as the L3 devices will not interfere with any communication on these lines as long as L3MODE remains HIGH (e.g. the L3CLK and L3DATA lines are normally connected to USART circuits in the microcontrollers which allow for convenient communication between microcontrollers).

Any addressing mode with a valid L3 operational address will re-enable the communication with the corresponding device.

Devices with a fixed operational address (‘Primary L3 devices’) will react with a device reset condition regardless of the state of DOM1 and DOM0.

Devices with a programmable operational address (‘Secondary L3 devices’) can only be put in the interface reset condition if the DOM1 and DOM0 bits are ‘0’. Other combinations of DOM1 and DOM0 initiate data transfers for ‘extended addressing’.

8.1.3 Extended addressing

L3 Devices with a programmable address can be informed of their operational address using a special data transfer.

8.1.3.1 Operational address declaration

For the declaration (programming) of the operational address of an L3 device with a ‘secondary L3 identification code’ the following actions are required:

1. First the microcontroller must issue an L3 operational address ‘000000’ (special function address) with DOM1 = 0 and DOM0 = 1. This combination defines the operational address declaration operation. Next the microcontroller will start a data transfer mode in which it first sends the secondary L3 identification code for the device that is to be issued an operational address, followed by a byte containing the operational address (the DOM bits in this byte are don't cares).
2. Next the microcontroller will start a data transfer mode in which it first sends the secondary L3 identification code for the device that is to be issued an operational address, followed by a byte containing the operational address (the DOM bits in this byte are don't cares).

A secondary L3 identification code is unique for any design. Devices of the same design have the same identification code of one or more bytes. However, special designs may have a range of identification codes, one of which can be selected by a hardware solution, to enable the connection of more than one device of the same design to the L3 interface. It is also possible to use separate L3MODE lines for multiple devices of the same design, but the same L3 identification code (this also enables ‘parallel programming’ of these devices). Bit 0 of any identification code byte will indicate whether or not an additional byte follows:

Bit 0 = 0; no additional byte as part of the identification code.

Bit 0 = 1; additional byte follows.

With this the number of secondary L3 identification codes is (theoretically) unlimited.

The operational address for the programmable device is preferable in the range 111000 to 111111. However, it is possible in a given application to issue any operational address that is not used to address primary L3 devices or other secondary L3 devices. An example is given in Table 36.

Table 36 Example of L3 devices; notes 1 to 4

ADDRESSING MODE	DATA MODE			
SPECIAL ADDRESS	SECONDARY L3 IDENTIFICATION CODE			OPERATIONAL ADDRESS (ONE BYTE)
	BYTE 1	BYTE 2	BYTE 3	
10000000	1XXXXXXX	1XXXXXXX	0XXXXXXXX	MMYYYYYY

Notes

1. Bits are shown in the order they appear on L3DATA (bit 0 first, bit 7 last).
2. X = bit of the identification code.
3. M = DOM bit of operational address (don’t care).
4. Y = bit of the operational address.

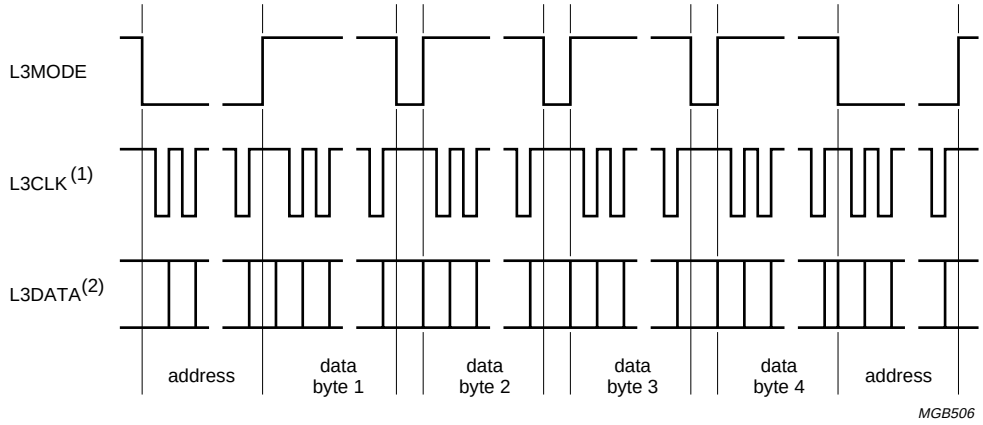
8.1.3.2 Operational address invalidation

In order to re-allocate an operational address that has been allocated to a secondary L3 device it is possible to invalidate an operational address:

- First the microcontroller must issue an L3 operational address ‘000000’ (special function address) with DOM1 = 1 and DOM0 = 0. This combination defines the operational address invalidation operation.
- Next the microcontroller will start a data transfer mode in which it only sends the secondary L3 identification code for the device that will no longer be addressed. From this moment on the device will not be able to communicate with the microcontroller until it is issued a new operational address by an OA declaration (it will enter a ‘device interface reset’ condition).

Remark: the combination of a special function address (000000) and DOM1 and DOM0 equal to ‘1’ is reserved for future applications. Designs based on this specification will react with a ‘device interface reset’.

8.1.4 EXAMPLE OF A DATA TRANSFER



(1) L3CLK is triggered by L3MODE.
(2) For more details (see Fig.20).

Fig.18 Example of transfer of 4 bytes.

A data transfer starts when the microcontroller sends an address on the bus. All ICs will evaluate this address, but only the IC addressed will be an active partner for the microcontroller in the following data transfer mode.

During the data transfer mode bytes will be sent from or to the microcontroller. In this example the L3MODE line is made LOW (‘halt mode’) in between byte transfers. This is the default operation, although some ICs may allow the L3MODE line to be kept HIGH. This exception must be specified clearly in the IC documentation, and such ICs must be able to communicate with microcontrollers that make L3MODE LOW in between transfers. It is suggested that new designs only use bytes as basic data transfer units. After the data transfer the microcontroller does not need to send a new address until a new data transfer is necessary. Alternatively it may also send the ‘special address’ 000000 to indicate the end of the data transfer operation.

8.1.5 TIMING REQUIREMENTS

These are requirements for the slave devices designed according to the 'L3' interface definitions.

8.1.5.1 Addressing mode

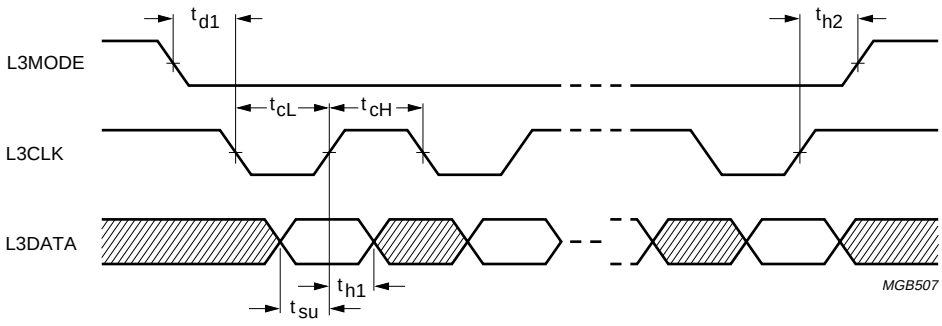


Fig.19 Addressing mode timing.

Table 37 Requirements for addressing mode timing (see Fig.19)

SYMBOL	PARAMETER	REQUIREMENT	UNIT
t_{d1}	L3CLK HIGH to L3CLK LOW delay time after L3MODE LOW	≥190	ns
t_{cL}	L3CLK LOW time	≥250	ns
t_{cH}	L3CLK HIGH time	≥250	ns
t_{su1}	L3DATA set-up time before L3CLK HIGH	≥190	ns
t_{h1}	L3DATA hold time after L3CLK HIGH	≥30	ns
t_{h2}	L3CLK hold time before L3MODE HIGH	≥190	ns

8.1.5.2 Data mode

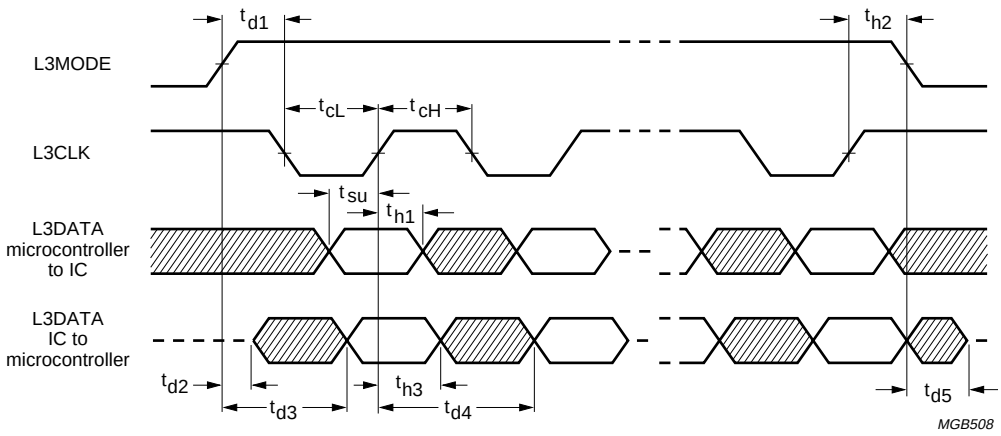


Fig.20 Data mode timing.

Table 38 Requirements for data mode timing (see Fig.20)

SYMBOL	PARAMETER	REQUIREMENT	UNIT
t_{d1}	L3CLK HIGH to L3CLK LOW delay time after L3MODE HIGH	≥190	ns
t_{cL}	L3CLK LOW time	≥250	ns
t_{cH}	L3CLK HIGH time	≥250	ns
Microcontroller to slave device			
t_{su1}	L3DATA set-up time before L3CLK HIGH	≥190	ns
t_{h1}	L3DATA hold time after L3CLK HIGH	≥30	ns
t_{h2}	L3CLK hold time before L3MODE HIGH	≥190	ns
Slave device to microcontroller			
t_{d2}	L3DATA enable time after L3MODE HIGH	$0 < t_{d2} \leq 50$	ns
t_{d3}	L3DATA stable time after L3MODE HIGH	≤380	ns
t_{h3}	L3DATA hold time after L3CLK HIGH	≥50	ns
t_{d4}	L3DATA stable time after L3CLK HIGH	≤360	ns
t_{d4}	L3DATA stable time after L3CLK HIGH between bit 7 of a byte and bit 0 of next byte if no halt mode is used	≤530	ns
t_{d5}	L3DATA disable time after L3MODE LOW	$0 < t_{d5} \leq 50$	ns

8.1.5.3 Halt mode

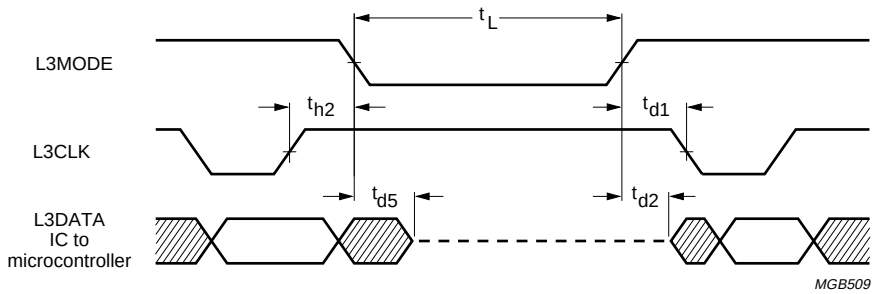


Fig.21 Halt mode timing.

Table 39 Requirements for halt mode timing (see Fig.21)

SYMBOL	PARAMETER	REQUIREMENT	UNIT
t_{d1}	L3CLK HIGH to L3CLK LOW delay time after L3MODE HIGH	≥190	ns
t_L	L3MODE LOW time	≥190	ns
t_{h2}	L3CLK hold time before L3MODE LOW	≥190	ns
Slave device to microcontroller			
t_{d2}	L3DATA enable time after L3MODE HIGH	$0 < t_{d2} \leq 50$	ns
t_{d5}	L3DATA disable time after L3MODE LOW	$0 < t_{d5} \leq 50$	ns

8.2 SAA2501 L3 protocol enhancement options

The L3 interface on the SAA2501 is limited in speed, dictated both by the maximum SAA2501 handling speed and the upper frequencies of the L3 interfacing standard. On the other hand, the SAA2501 offers several enhancements to make a better use of the SAA2501 L3 interface capacity. The enhancements are optional. The applicant chooses whether to use them or not.

8.2.1 Testing L3RDY by polling L3DATA

The host must test status flag L3RDY to make sure whether the SAA2501 L3 interface is ready to transfer data item bytes. According to the general protocol, described in Section 7.20.6, the status is read by first writing the SAA2501 ‘read status’ operational address, after which the status byte can be transferred. To avoid these status byte transfers (thus reducing the host's load), after writing the SAA2501 ‘read status’ operational address, L3RDY is continuously copied to signal L3DATA during the period in which no L3 transfers (i.e. status byte readings) are performed. Meanwhile, L3MODE must be kept HIGH (no L3 operational addresses may be written). As a result, L3RDY can be tested as shown in Table 40.

Table 40 Testing L3RDY by polling L3DATA; note 1

L3DATA	TRANSFER SOURCE	L3MODE	EXPLANATION
01100011	host	0	write ‘read status’ operational address
polled	SAA2501	1	test L3DATA; repeat this step until L3DATA = 1

Note

1. No status byte transfers are needed; the load of the host (microcontroller) can thus be reduced.

8.2.2 Options to increase the timing accuracy of the APU coefficient writing

The SAA2501 offers three enhancements to increase the timing accuracy with which APU coefficients can be updated by the application:

1. Status polling is not required when APU coefficients are written. L3 status flag L3RDY, when read anyhow, will always be HIGH, indicating that the next APU coefficient transfer may be done. The transfer speed is only limited by the maximum allowed frequency of L3CLK. As a result, also no ‘write item data’ operational address is needed any more before writing each APU coefficient index.
2. Normally, no more bytes may be written to a writeable data item than the length of that specific item. An exception is formed by the APU coefficients. They may be written continuously with a coefficient wrap. After the writing of all 4 coefficients, the writing can be continued at the first APU coefficient without having to write a new control byte.
3. The data item transfer protocol, described in Section 7.20.6, although transparent, allows only for the reading or writing of data items from their first data byte onwards. This approach can lead to situations where e.g. 54 Ancillary Data item bytes must all be read (which takes at least $54 \times 200\ \mu s = 10.8$ ms, due to the interface speed limitations: see Section 7.20.6) before the next data item can be transferred. The SAA2501 enables the writing of APU coefficients without having to wait for the current item transfer to finish. In order to do so, a running transfer can be interrupted by an APU coefficient write transfer, and then be resumed with the ‘continue current transfer’ control byte.

   An item transfer may be interrupted at any time to write APU coefficients. After the ‘continue previous transfer’ control byte, a operational address must always follow, indicating the type of L3 transfer that will follow. An APU coefficient write transfer itself cannot be interrupted.

The 3 mentioned options are all illustrated in Table 41, where a data item transfer is interrupted between the reading of the n^{th} and $(n + 1)^{th}$ data item byte.

Table 41 Example of 3 options to increase the timing accuracy of the APU coefficient writing

L3DATA(1)	TRANSFER SOURCE	L3MODE	EXPLANATION
DDDDDDDD	SAA2501	1	read n^{th} item data byte
01100010	host	0	indicate ‘write control’ transfer
00000110	host	1	write ‘write APU coefficients’ control byte
01100000	host	0	indicate ‘write item data’ transfer
DDDDDDDD	host	1	write APU coefficient LL
DDDDDDDD	host	1	write APU coefficient LR
DDDDDDDD	host	1	write APU coefficient RL
DDDDDDDD	host	1	write APU coefficient RR
DDDDDDDD	host	1	write APU coefficient LL
DDDDDDDD	host	1	write APU coefficient LR
DDDDDDDD	host	1	write APU coefficient RL
DDDDDDDD	host	1	write APU coefficient RR
01100010	host	0	indicate ‘write control’ transfer
00000111	host	1	write ‘continue previous transfer’ control byte
01100011	host	0	indicate ‘read status’ transfer
SSSSSSSS	SAA2501	1	read status; repeat this step until L3RDY = 1
01100001	host	0	indicate ‘read item data’ transfer
DDDDDDDD	SAA2501	1	read $(n + 1)^{th}$ item data byte
etc.	etc.	etc.	etc.

Note

1. Explanation of bytes:
   a) DDDDDDDD = data byte.
   b) SSSSSSSS = status byte.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.5	+6.5	V
V_I	input voltage	note 1	–0.5	V_{DD} + 0.5	V
I_{DD}	supply current		–	100	mA
I_I	input current		–	10	mA
I_O	output current	2 mA outputs	–	10	mA
		4 mA outputs	–	20	mA
P_{tot}	total power dissipation	VDD = 5 V±5%	–	165	mW
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es1}	electrostatic handling	note 2	–2000	+2000	V
V_{es2}	electrostatic handling	note 3	–200	+200	V

Notes

1. Input voltage should not exceed 6.5 V unless otherwise specified.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

10 DC CHARACTERISTICS

V_{DD} = 5 V ±10%; T_{amb} = −40 to +85 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_{DD}	quiescent supply current	note 1	100	–	–	μA
Inputs; notes 2 and 3						
V_{IH}	HIGH level input voltage (CMOS)		$0.7V_{DD}$	–	V_{DD}	V
V_{IL}	LOW level input voltage (CMOS)		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage (TTL)		2	–	V_{DD}	V
V_{IL}	LOW level input voltage (TTL)		0	–	0.8	V
V_{tLH}	positive going threshold voltage (CMOS Schmitt trigger)		–	–	$0.8V_{DD}$	V
V_{tHL}	negative going threshold voltage (CMOS Schmitt trigger)		$0.2V_{DD}$	–	–	V
V_{hys}	hysteresis voltage (CMOS Schmitt trigger)		–	$0.3V_{DD}$	–	V
$\|I_I\|$	input current		–	–	5	μA
R_{pull}	pull-up resistor		14	–	140	kΩ
Outputs						
V_{OH}	HIGH level output voltage	I_O = 4 mA	V_{DD} − 0.5	–	–	V
V_{OL}	LOW level output voltage	I_O = 4 mA	–	–	0.5	V
$\|I_{OZ}\|$	3-state OFF-state leakage current		–	–	5	μA

Notes

1. TDI, TMS, TRST and L3DATA not driven; TC0 and TC1 driven HIGH; all other inputs driven LOW.
2. Inputs TRST, TCK, TMS and TDI are TTL level compatible; all other inputs are CMOS level compatible.
3. Input TRST (pin 38) should be connected to ground for normal operation and connected to V_{DD} for boundary scan testing.

11 AC CHARACTERISTICS

V_{DD} = 5 V ±10%; T_{amb} = −40 to +85 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clocks						
C_i	input capacitance		–	–	10	pF
MCLKIN						
f_{clk}	clock frequency	MCLK24 = 1	–	24.576	–	MHz
		MCLK24 = 0	–	12.288	–	MHz
t_r	rise time		–	12	–	ns
t_f	fall time		–	12	–	ns
t_H	HIGH time		12	–	–	ns
t_L	LOW time		12	–	–	ns
X22IN						
f_{clk}	clock frequency		–	22.579	–	MHz
t_r	rise time		–	12	–	ns
t_f	fall time		–	12	–	ns
t_H	HIGH time		12	–	–	ns
t_L	LOW time		12	–	–	ns
FSCLKIN						
f_{clk}	clock frequency	FSCLK384 = 1	–	$384f_s$	–	Hz
		FSCLK384 = 0	–	$256f_s$	–	Hz
t_r	rise time	note 1	–	5	–	ns
t_f	fall time	note 1	–	5	–	ns
t_H	HIGH time		12	–	–	ns
t_L	LOW time		12	–	–	ns
CDSCL						
f_{clk}	clock frequency		–	–	768	kHz
t_r	rise time	note 1	–	12	–	ns
t_f	fall time	note 1	–	12	–	ns
t_H	HIGH time	note 2	T_m + 20	–	–	ns
t_L	LOW time	note 2	T_m + 20	–	–	ns
CDMCL						
f_{clk}	clock frequency	note 2	–	$\frac{1}{8T_m}$	–	Hz
L3CLK						
t_H	HIGH time		T_m + 10	–	–	ns
t_L	LOW time		T_m + 10	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FSCLK						
f_{clk}	clock frequency	MSEL = 00; FSCLKM = 0; f_s = 44.1 kHz	–	$\frac{1}{2}f_{X22IN}$	–	MHz
		MSEL = 00; FSCLKM = 0; f_s = 48 kHz	–	$\frac{1}{2}f_{MCLKIN}$	–	MHz
		MSEL = 00; FSCLKM = 0; f_s = 32 kHz	–	$\frac{1}{3}f_{MCLKIN}$	–	MHz
MCLK						
f_{clk}	clock frequency		–	f_{MCLKIN}	–	MHz
SCK						
f_{clk}	clock frequency	FSCLK384 = 0; $f_{SCK} = 64f_s$	–	$\frac{1}{4}f_{SCLK}$	–	MHz
		FSCLK384 = 1; $f_{SCK} = 64f_s$	–	$\frac{1}{6}f_{SCLK}$	–	MHz
Inputs						
C_i	input capacitance		–	–	10	pF
t_{su1}	set-up time FDAI to SCK HIGH	C_L < 25 pF	33	–	–	ns
t_{su2}	set-up time CDM and CDMEF to CDMCL, CDS, CDSEF and CDSWA HIGH	C_L < 25 pF	42	–	–	ns
t_{su3}	set-up time CDSSY to CDSCL HIGH		T_m + 10	–	–	ns
t_{d1}	delay time L3MODE to L3LCK LOW		0	–	–	ns
t_{h1}	hold time FDAI to SCK HIGH		0	–	–	ns
t_{h2}	hold time CDM, CDMEF to CDMCL, CDS, CDSEF and CDSWA HIGH		0	–	–	ns
t_{h3}	hold time CDSSY to CDSCL HIGH		10	–	–	ns
t_{h4}	input hold time		0	–	–	ns
t_L	L3MODE LOW time		T_m + 10	–	–	ns
Outputs						
C_o	output capacitance		–	–	50	pF
t_h	hold time SD, WS, FDAO, FDFSY and FDEF to SCK LOW	notes 3 and 4	–22	–	–	ns
t_h	hold time CDMWS to CDMCL LOW	notes 3 and 4	–15	–	–	ns
t_d	delay time SD, WS, FDAO, FDFSY and FDEF to CDMCL LOW	note 3	–	–	10	ns
t_d	delay time CDMWS to CDMCL LOW	note 3	–	–	0	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs/outputs						
C_o	output capacitance		–	–	50	pF
t_{su}	input set-up time	note 5	$T_m + 10$	–	–	ns
t_h	input hold time	note 5	10	–	–	ns
t_h	output hold time	notes 3 and 5	T_m	–	–	ns
t_d	output delay time	notes 3 and 5	–	–	$2T_m + 30$	ns
t_{d2}	3-state enable time	notes 3 and 6	–	–	20	ns
t_{d3}	3-state stable time	notes 3 and 6	–	–	20	ns
t_{d5}	3-state disable time L3DATA to L3MODE LOW	note 3	–	–	20	ns

Notes

1. Short rise and fall times improve the tolerance of clocks to signal and supply noise.
2. If MCLK24 = 1 then $T_m = \frac{4}{f_{MCLKIN}}$ else $T_m = \frac{2}{f_{MCLKIN}}$.
3. To allow for the effects of load capacitance the timing values should be de-rated by 0.5 ns/pF.
4. For maximum clock signal load of 25 pF.
5. L3DATA to L3CLK HIGH.
6. L3DATA to L3MODE HIGH.

12 APPLICATION INFORMATION

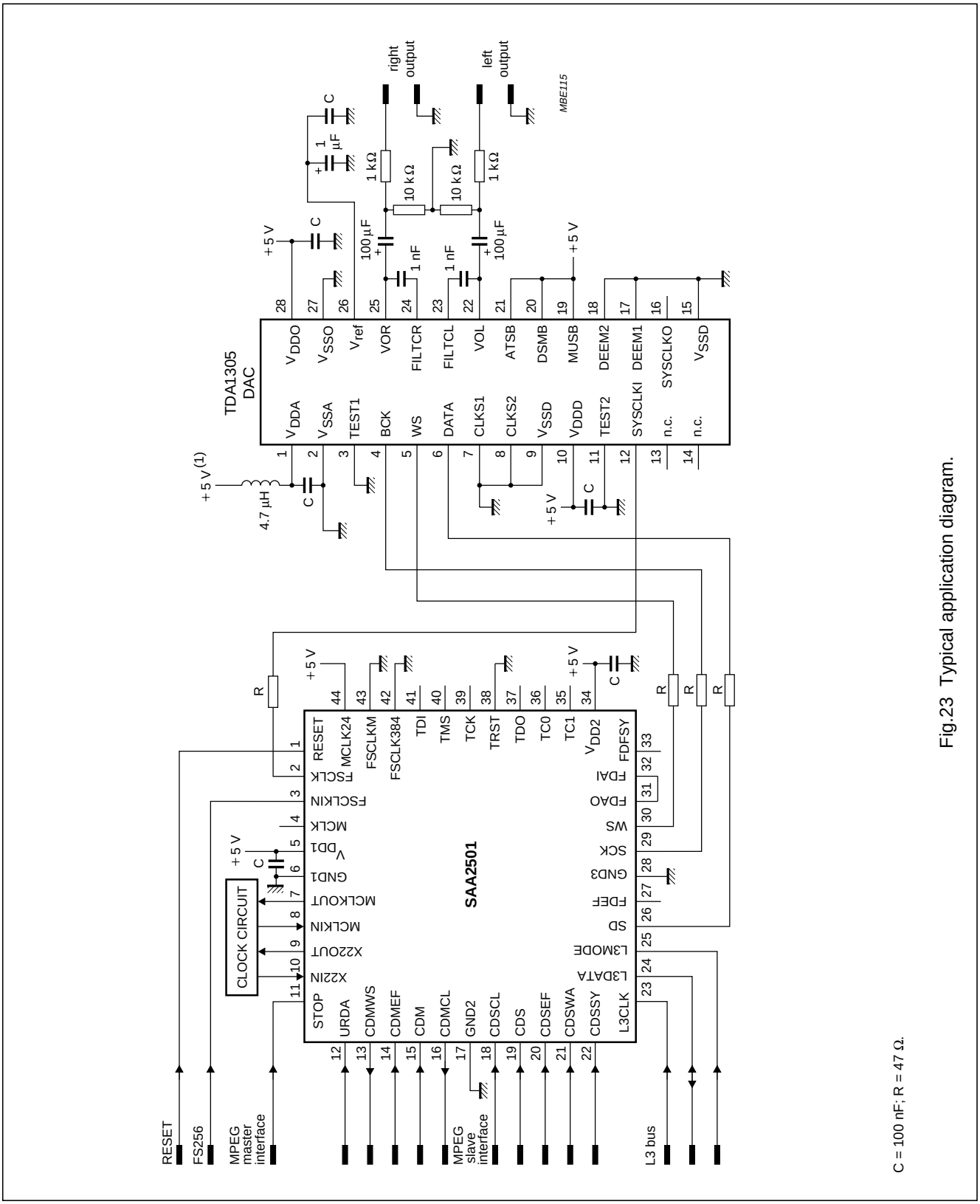
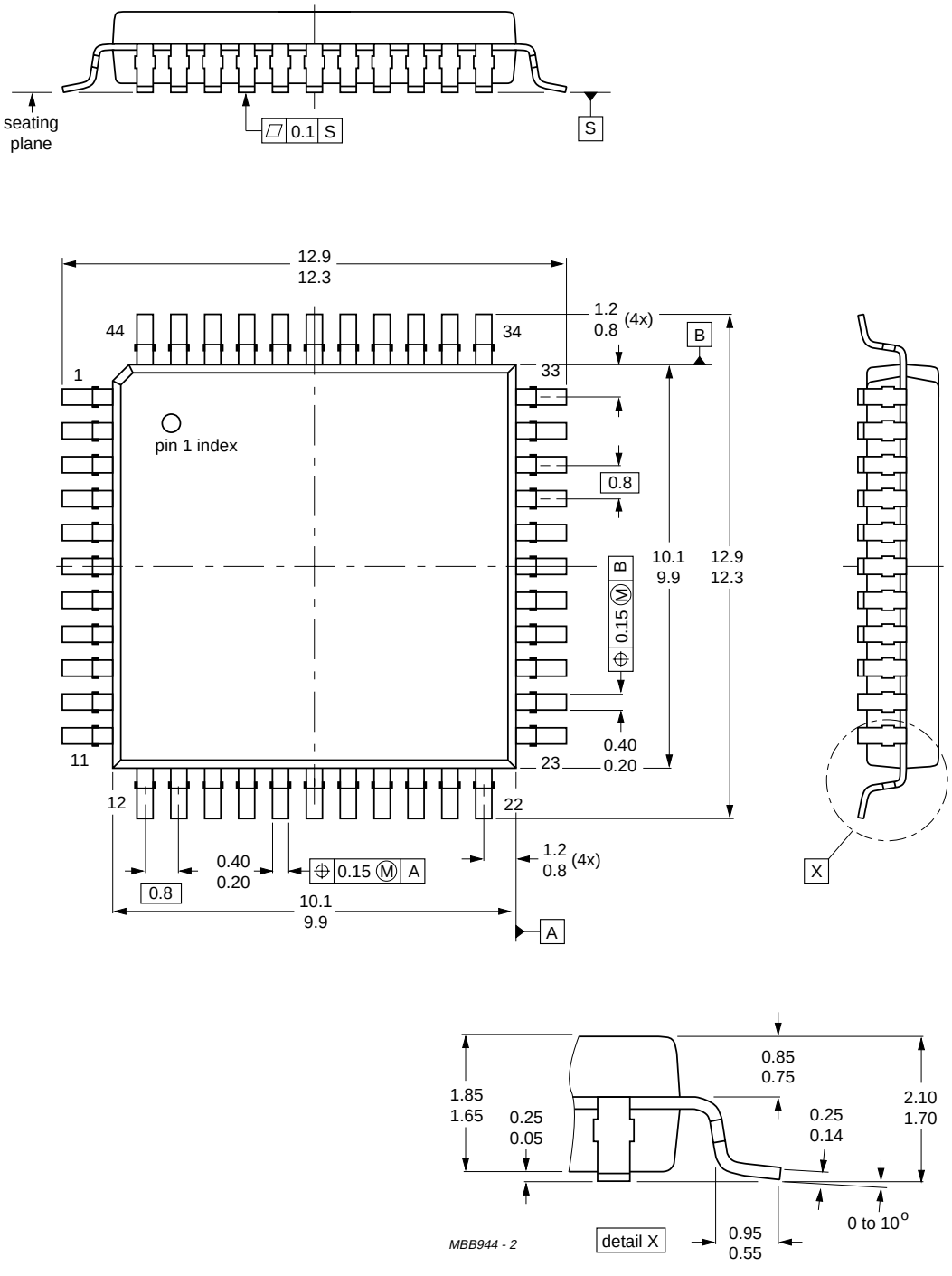


Fig.23 Typical application diagram.

13 PACKAGE OUTLINE



Dimensions in mm.

Fig.24 Plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm (QFP44; SOT307-2).

14 SOLDERING

14.1 Plastic quad flat-packs

14.1.1 BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

14.1.2 BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

14.1.3 REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

15 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

16 LIFE SUPPORT APPLICATIONS

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NOTES

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